

8

7

6

5

4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV

ZONE

ECN

DESCRIPTION OF CHANGE

CK APPD

ENG APPD

DATE

DATE

E

396944

PRODUCTION RELEASED

08/26/05

?

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REVISION HISTORY

43-46

SCHEMATIC CREF AND NETLIST REPORTS

SCHEM,MLB,PB15 "

08/25/2005

BOM OPTIONS (IN COMMON PARTS)

STUFF

NO STUFF

1_8V_MAXBUS

1_5V_MAXBUS

NO_SSCG

SSCG

5V_HD_LOGIC

3V_HD_LOGIC

NO_BBANG

BBANG

INT_2_5V_COLD

INT_2_5V_HOT

ATI_MEMIO_HI

ATI_MEMIO_LO

SOFT_MODEM

USB_MODEM

GPU_PWRMSR

EMI

GPU_SS

EXT_TMDS (BETTER/BEST)

VGA_BUFFER_RES

INT_TMDS (BEST128)

MMM

SUPERCAP

INT_TMDS (BETTER/BEST)

ADT7460

EXT_TMDS (BEST128)

BACKUP_BATT

ADT7467

PART#

QTY

DESCRIPTION

REFERENCE DESIGNATOR(S)

BOM OPTION

051-6680

1

SCHEM,MLB,PB15

SCH1

820-1679

1

PCBF,MLB,PB15

PCB1

826-4393

1

LABEL,PCB,28MM X 6MM

EEE:U3Z

LABEL_BST128

826-4393

1

LABEL,PCB,28MM X 6MM

EEE:U40

LABEL_BST64

826-4393

1

LABEL,PCB,28MM X 6MM

EEE:U41

LABEL_BTR

DIMENSIONS ARE IN MILLIMETERS

XX : _____

X.XX : _____

X.XXX : _____

ANGLES : _____

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER

ENG APPD

QA APPD

RELEASE

/

/

/

/

DESIGN CK

MFG APPD

DESIGNER

SCALE

/

/

/

NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

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SCHEM,MLB,PB15

DRAWING NUMBER 051-6680

REV. E

SHT 1 OF 46

8

7

6

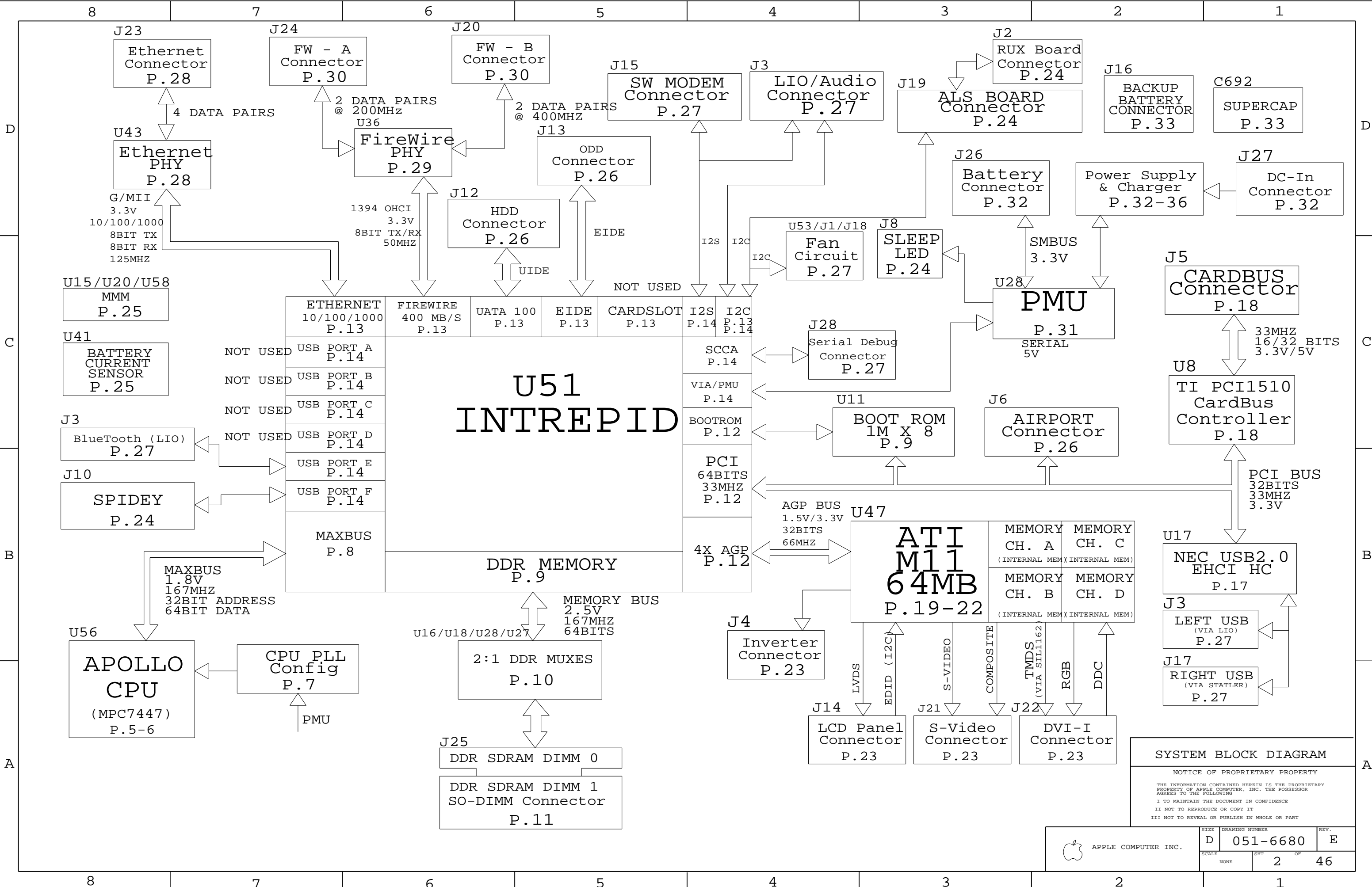
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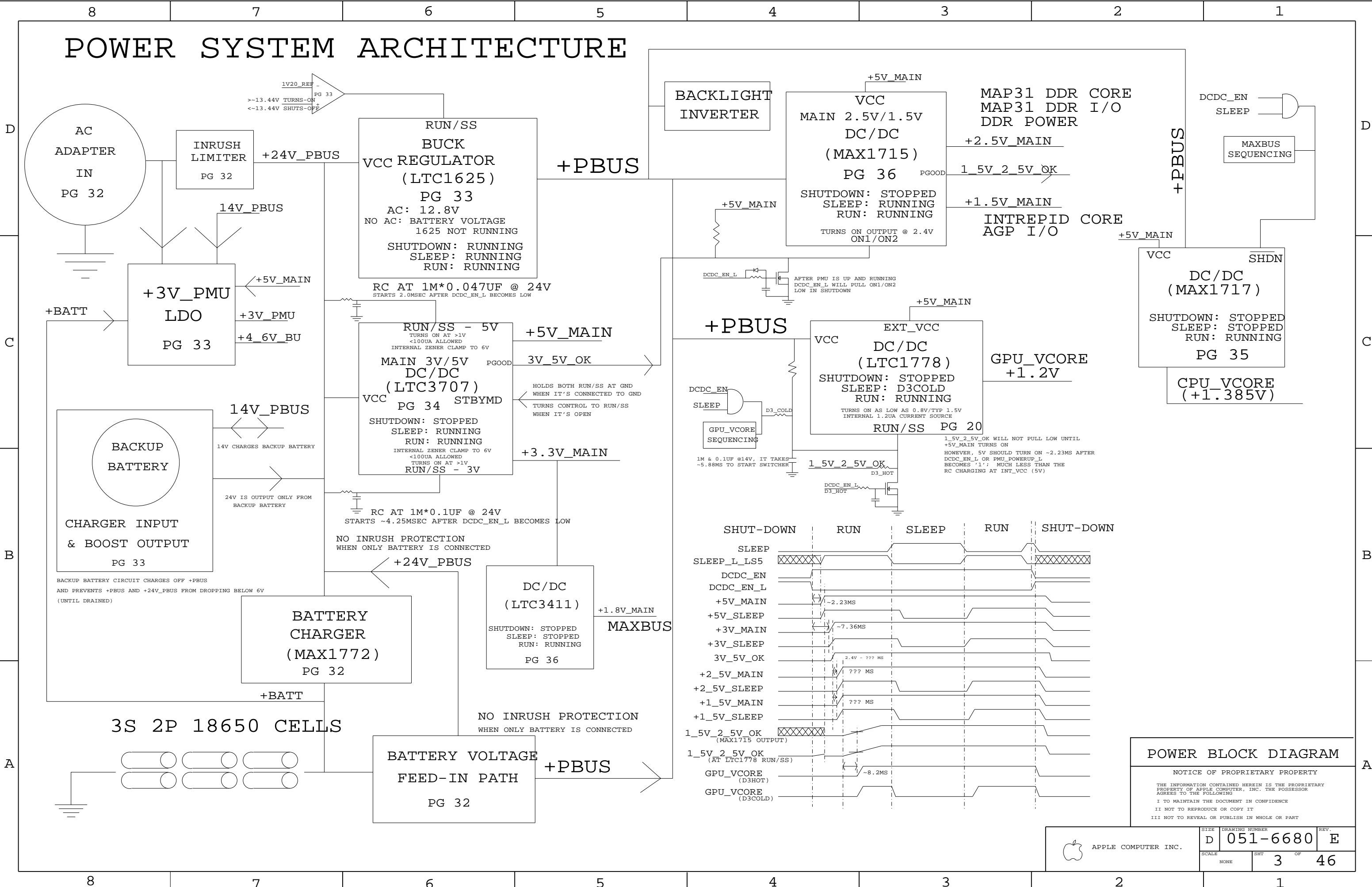
4

3

2

1





PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

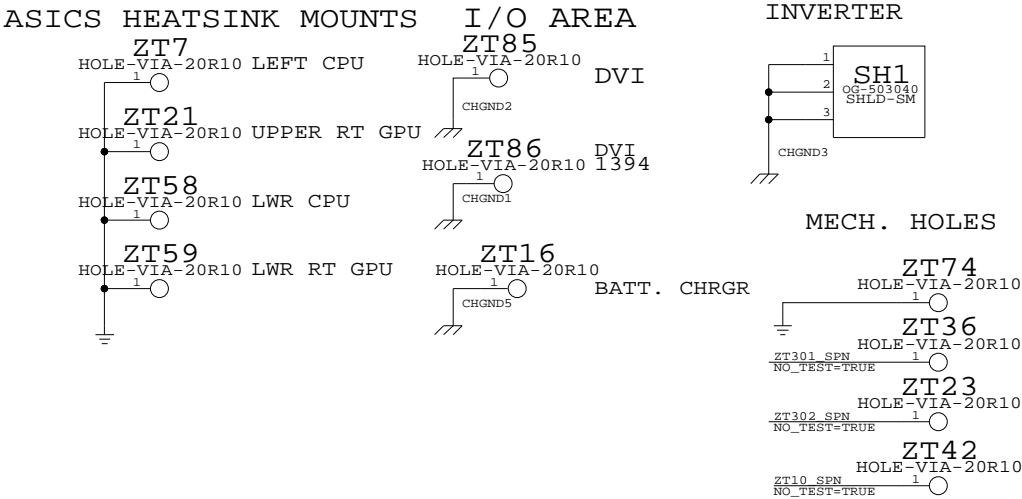
IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

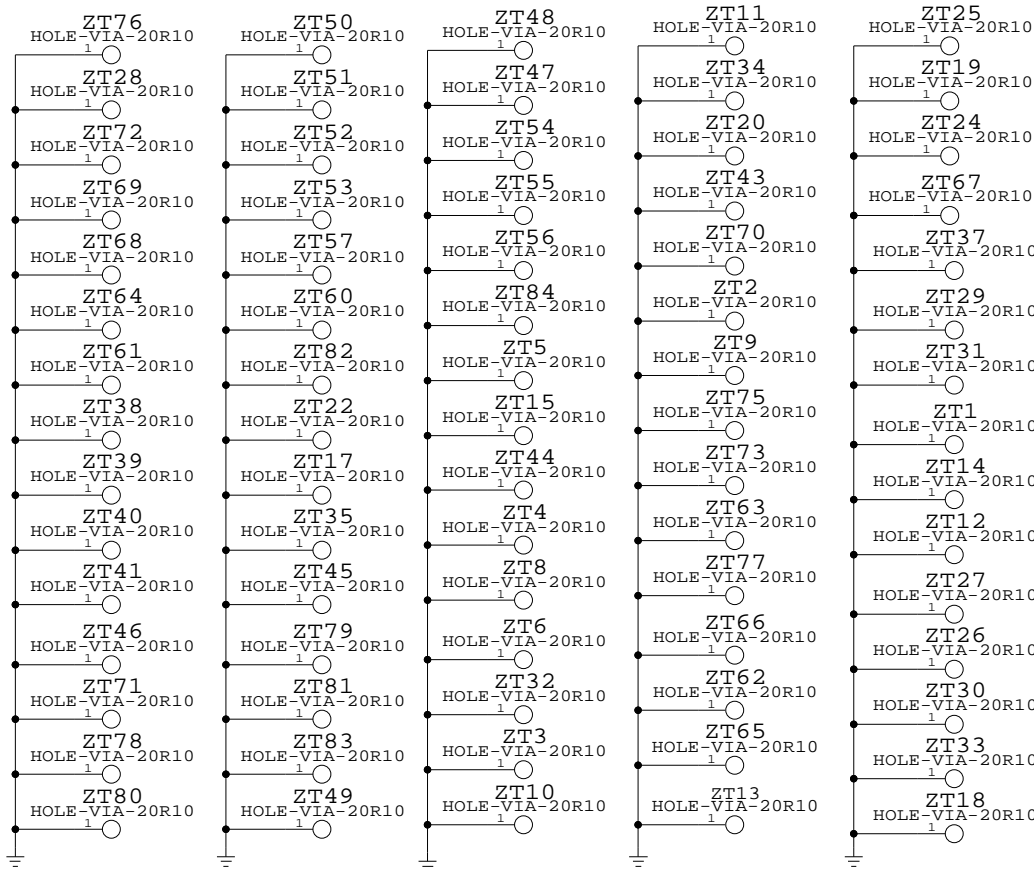
BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA				SIGNAL (1/2 OZ + COPPER PLATING)	
1				SIGNAL (1/2 OZ)	
2	PREPREG (3 MIL)			GROUND (1/2 OZ)	
3	PREPREG (3 MIL)			SIGNAL (1/2 OZ)	
4	CORE (3 MIL)			CUT POWER PLANE (1 OZ)	
5	PREPREG (5 MIL)			CUT POWER PLANE (1 OZ)	
6	CORE (5 MIL)			SIGNAL (1/2 OZ)	
7	PREPREG (5 MIL)			GROUND (1/2 OZ)	
8	CORE (3 MIL)			SIGNAL (1/2 OZ)	
9	PREPREG (3 MIL)			SIGNAL (1/2 OZ + COPPER PLATING)	
10	PREPREG (3 MIL)				

BOARD HOLES
CHASSIS MOUNTS



GROUND VIAS



BOARD INFORMATION

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SIZE	D	DRAWING NUMBER	051-6680	REV.	E
SCALE	NONE	SHT	4	OF	46

8	7	6	5	4	3	2	1
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2

1



B

B

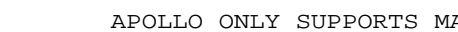


A

```

BUSTYPE  SELF
R110
22
43 7 6 5 CPU HRESET L 1 0 0 2 CPU EMODE0 L 0 0 0 0

```



SIGNAL	TIED	APPLICATION
U_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
	CPU_HRESET_L	2.5V INTERFACE
U_BUS_VSEL (PROCESSOR)	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION
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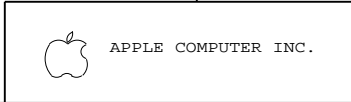
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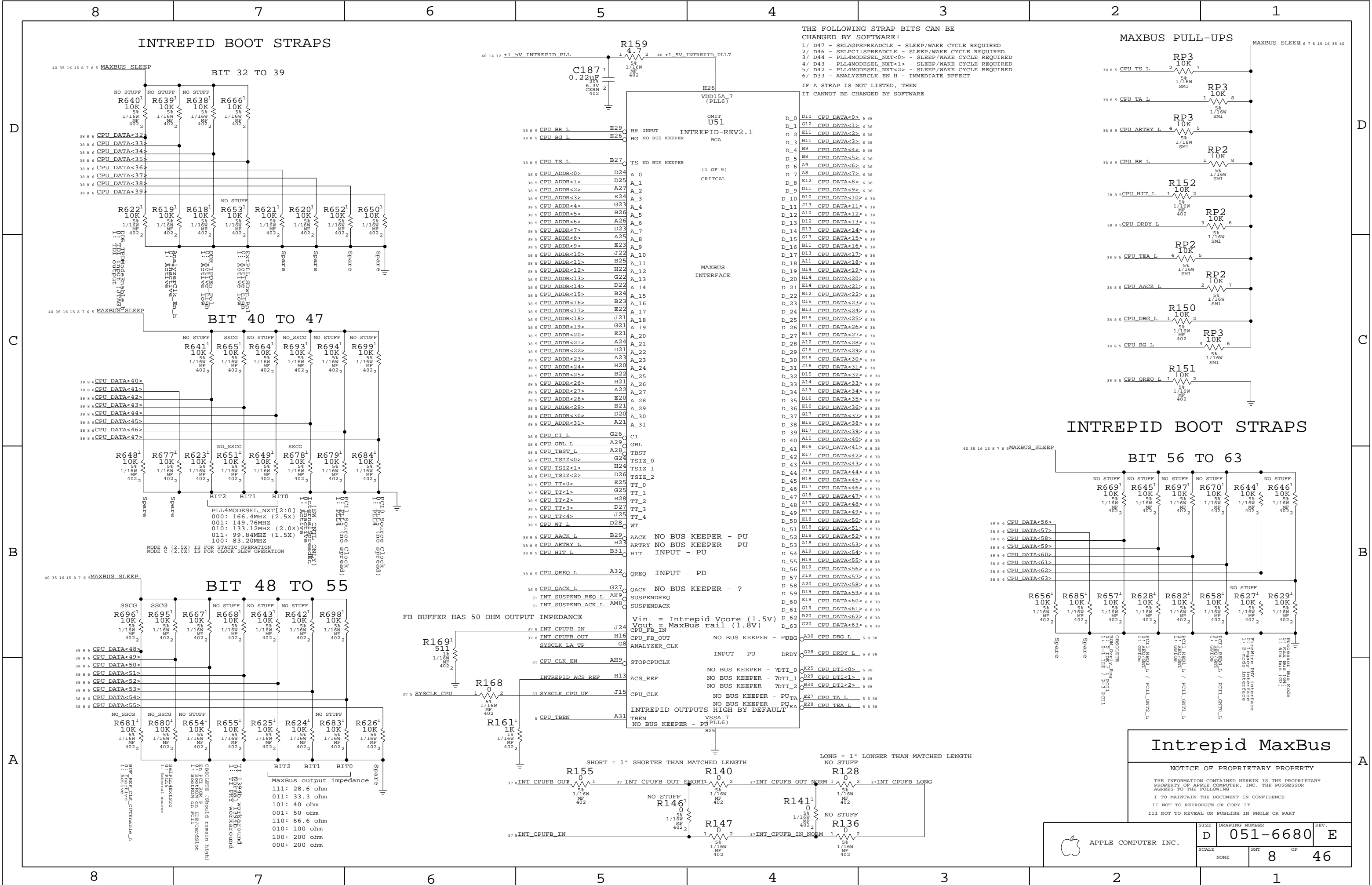
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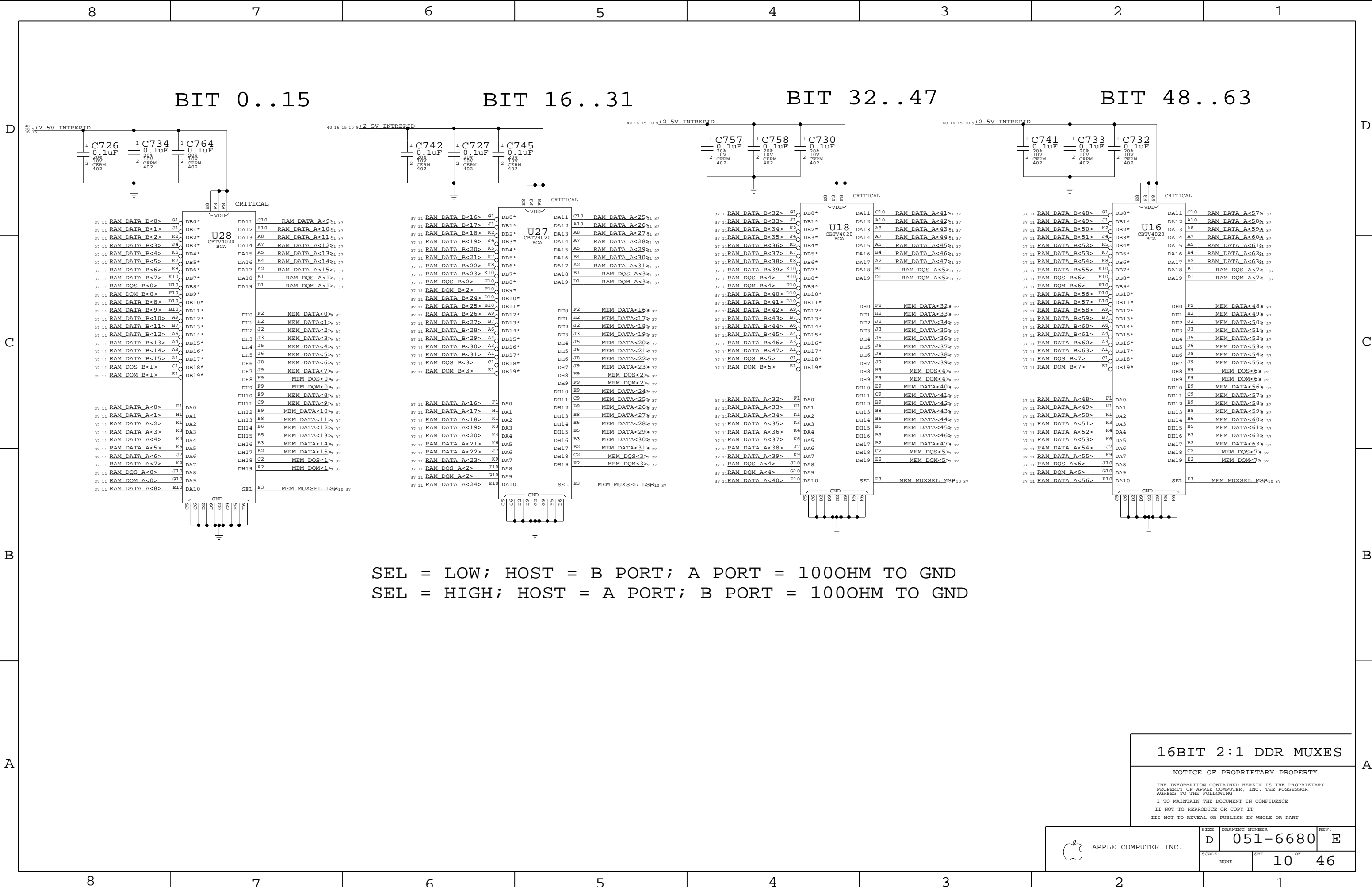


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SIZE	DRAWING NUMBER	REV.
D	051-6680	E

SCALE	SHT	OF
NONE	7	46





SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

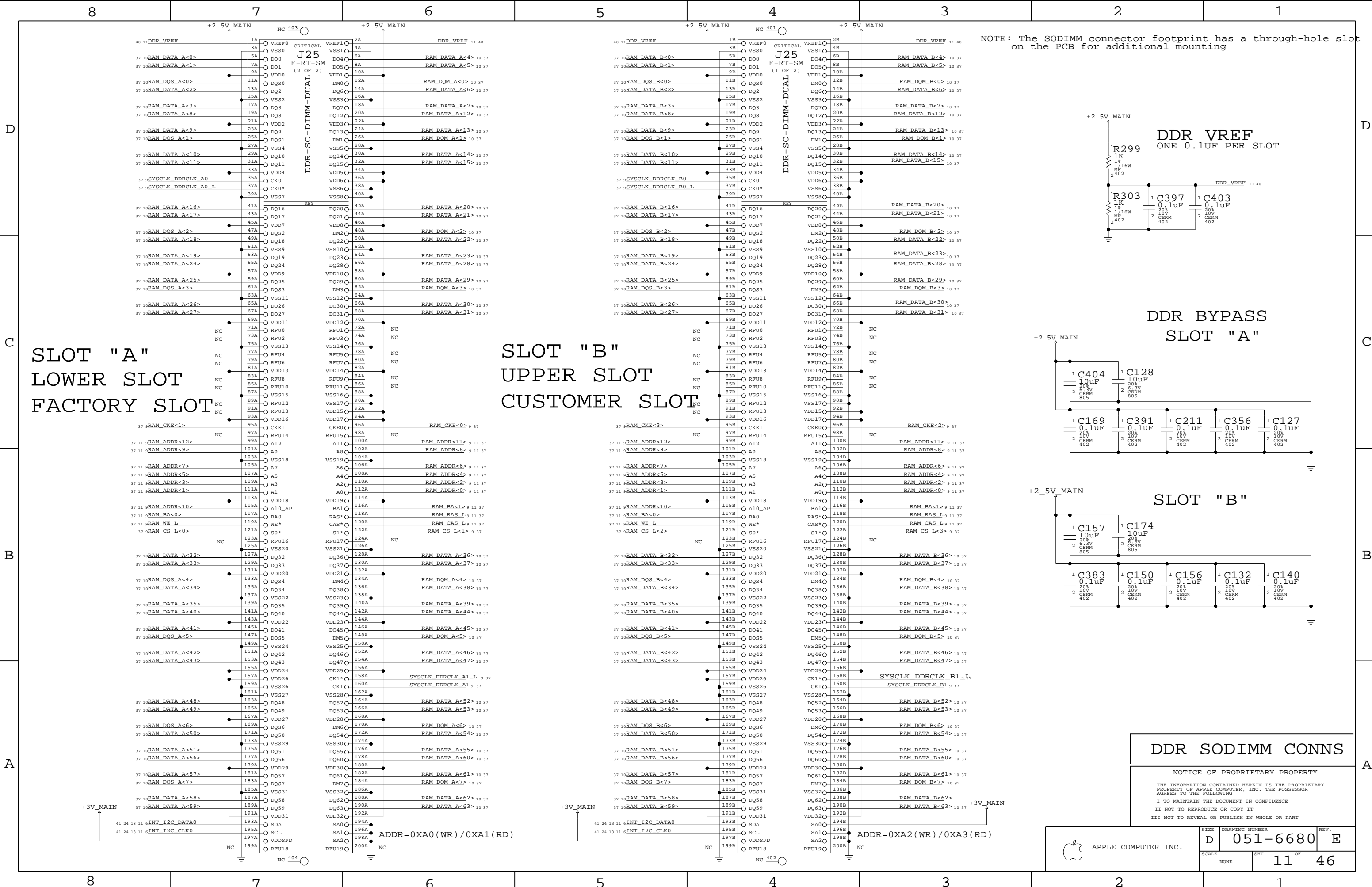
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SIZE	D	DRAWING NUMBER	051-6680	REV.	E
SCALE	NONE	SHT	10	OF	46



NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting

DDR VREF
ONE 0.1uF PER SLOT

DDR BYPASS
SLOT "A"

SLOT "B"

DDR SODIMM CONNS

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DRAWING NUMBER

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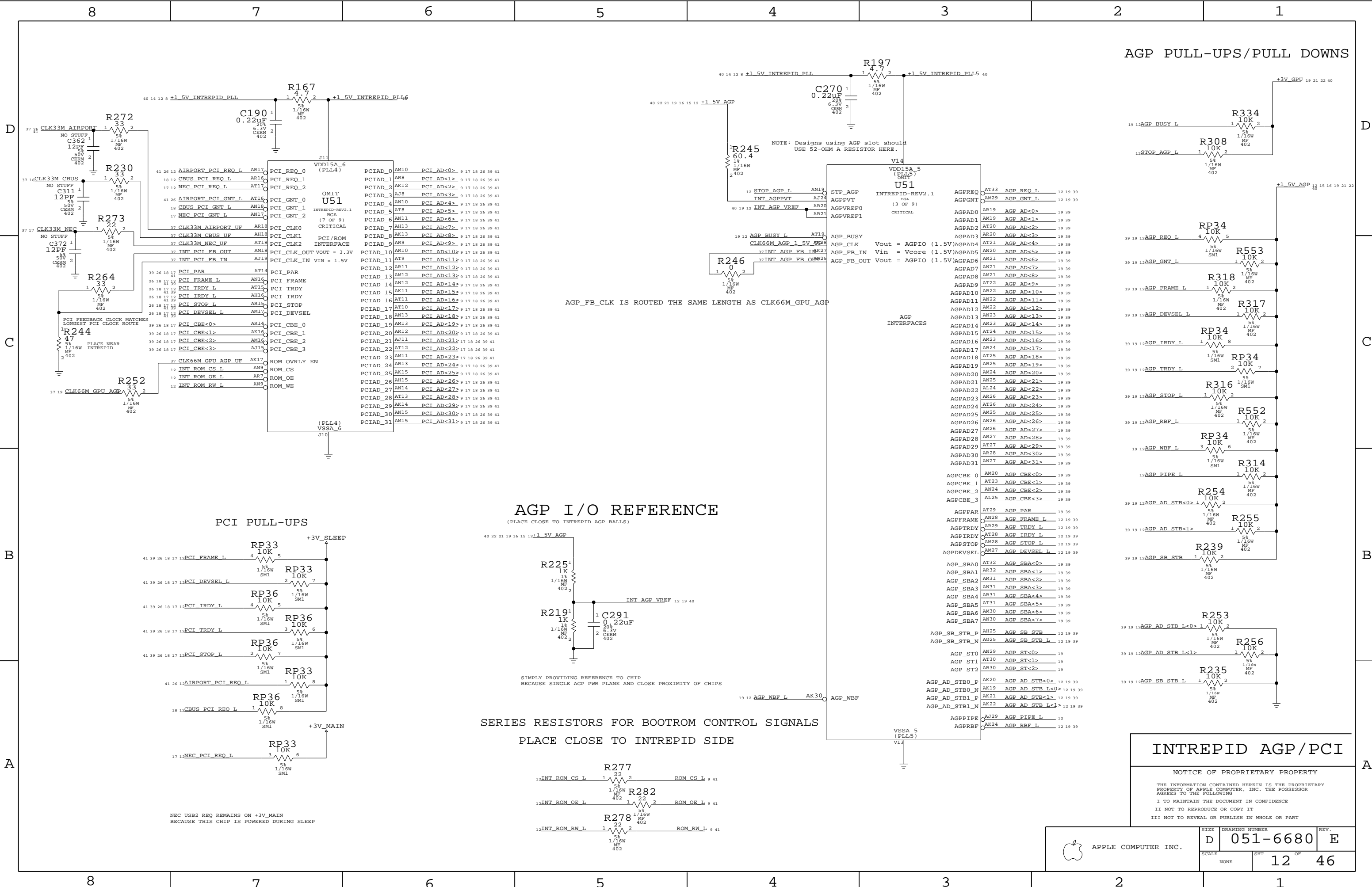
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SHT

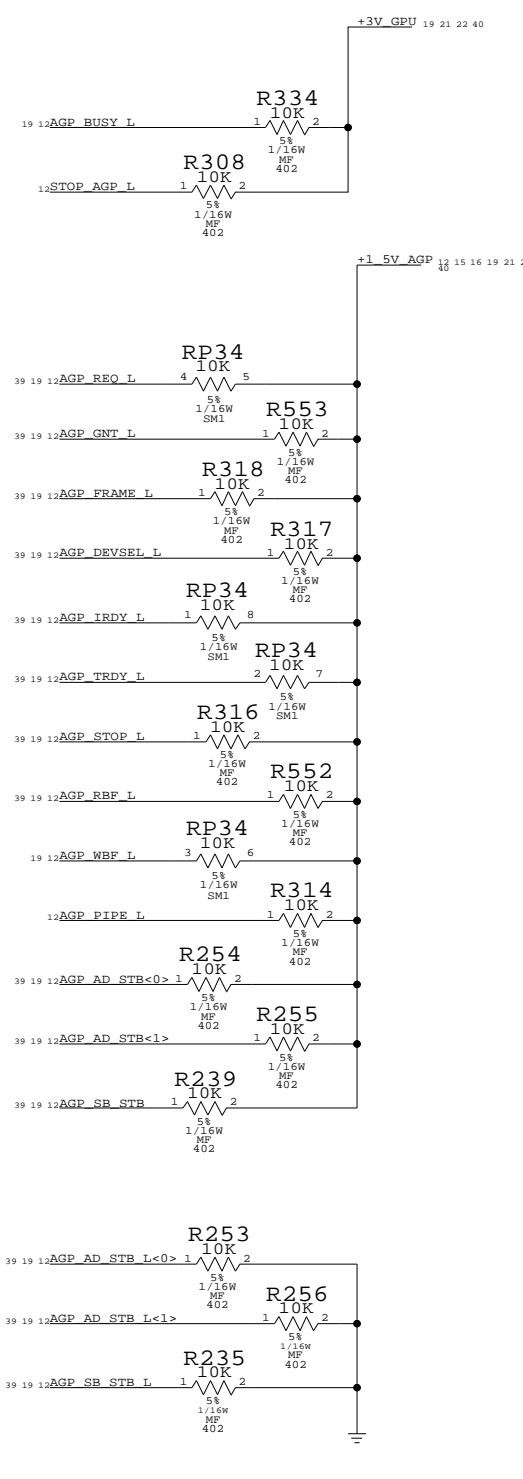
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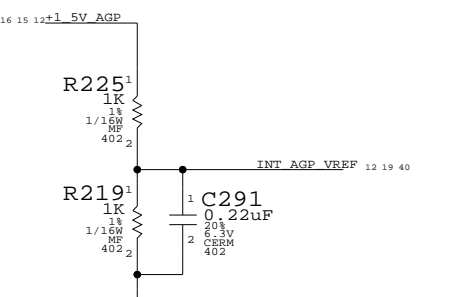
46



AGP PULL-UPS/PULL DOWNS

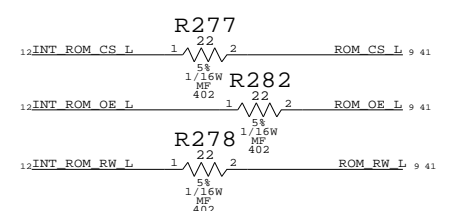


AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)



SIMPLY PROVIDING REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS
PLACE CLOSE TO INTREPID SIDE



INTREPID AGP/PCI

NOTICE OF PROPRIETARY PROPERTY

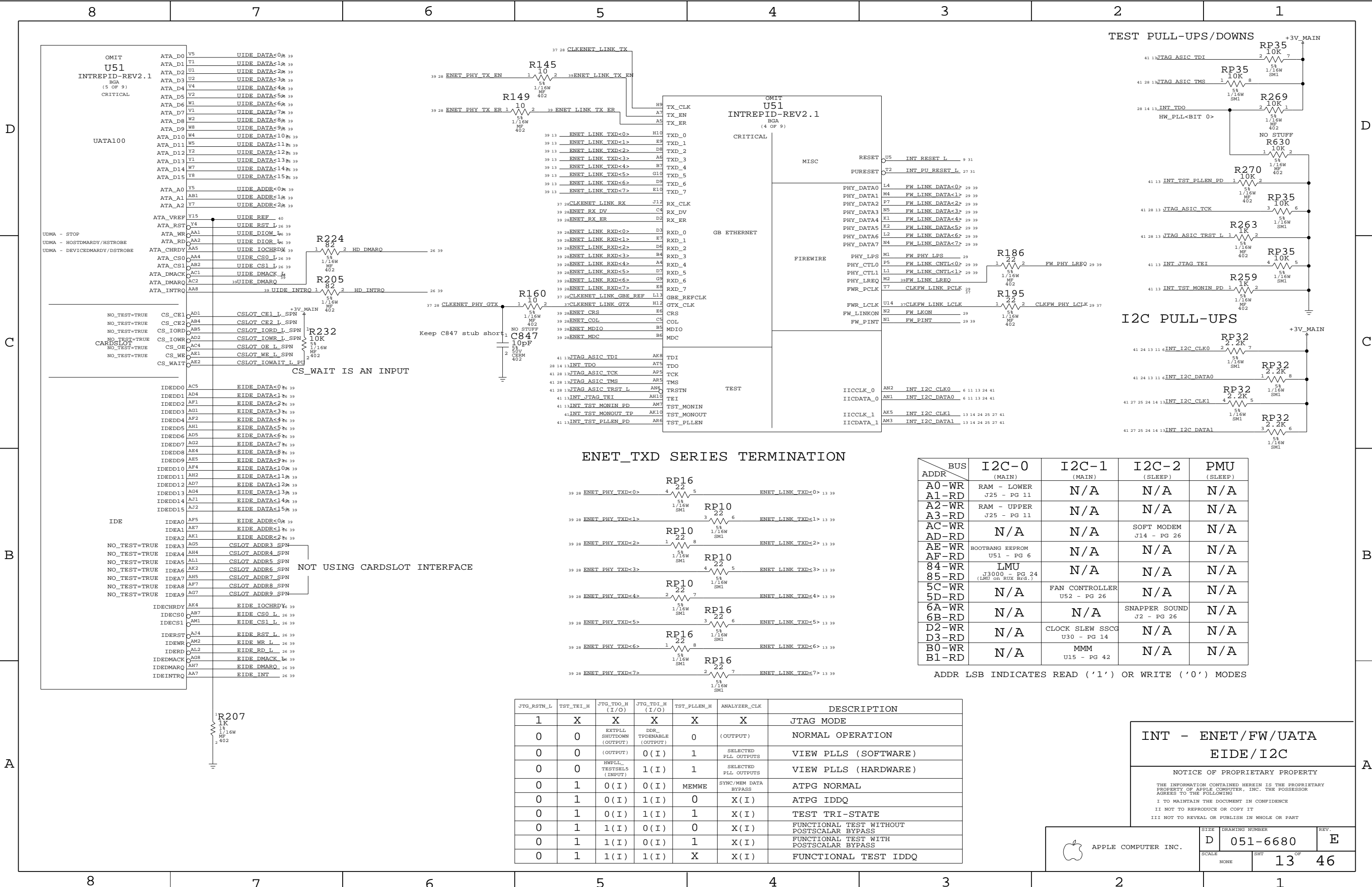
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	D	051-6680	E
SCALE	SHT		OF
	NONE		12 46



D

C

B

A

D

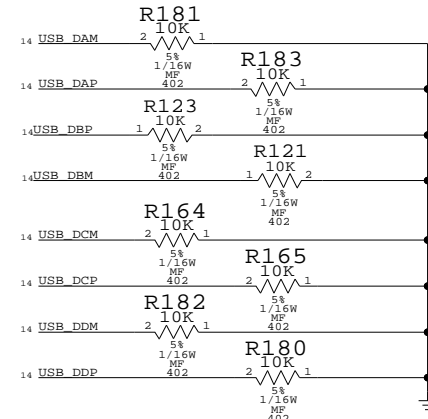
C

B

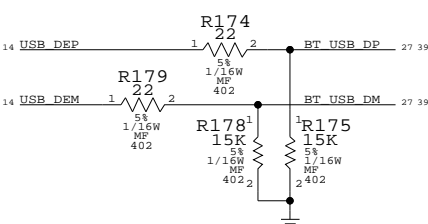
A

USB PORT ASSIGNMENTS

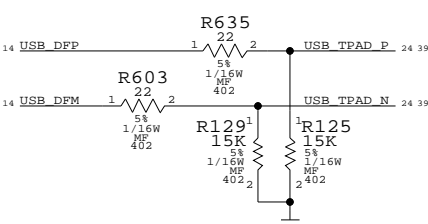
PORT A B C D/UNUSED



PORT E/BLEETOOTH



PORT F/TRACKPAD



INT - USB/GPIOS/I2S

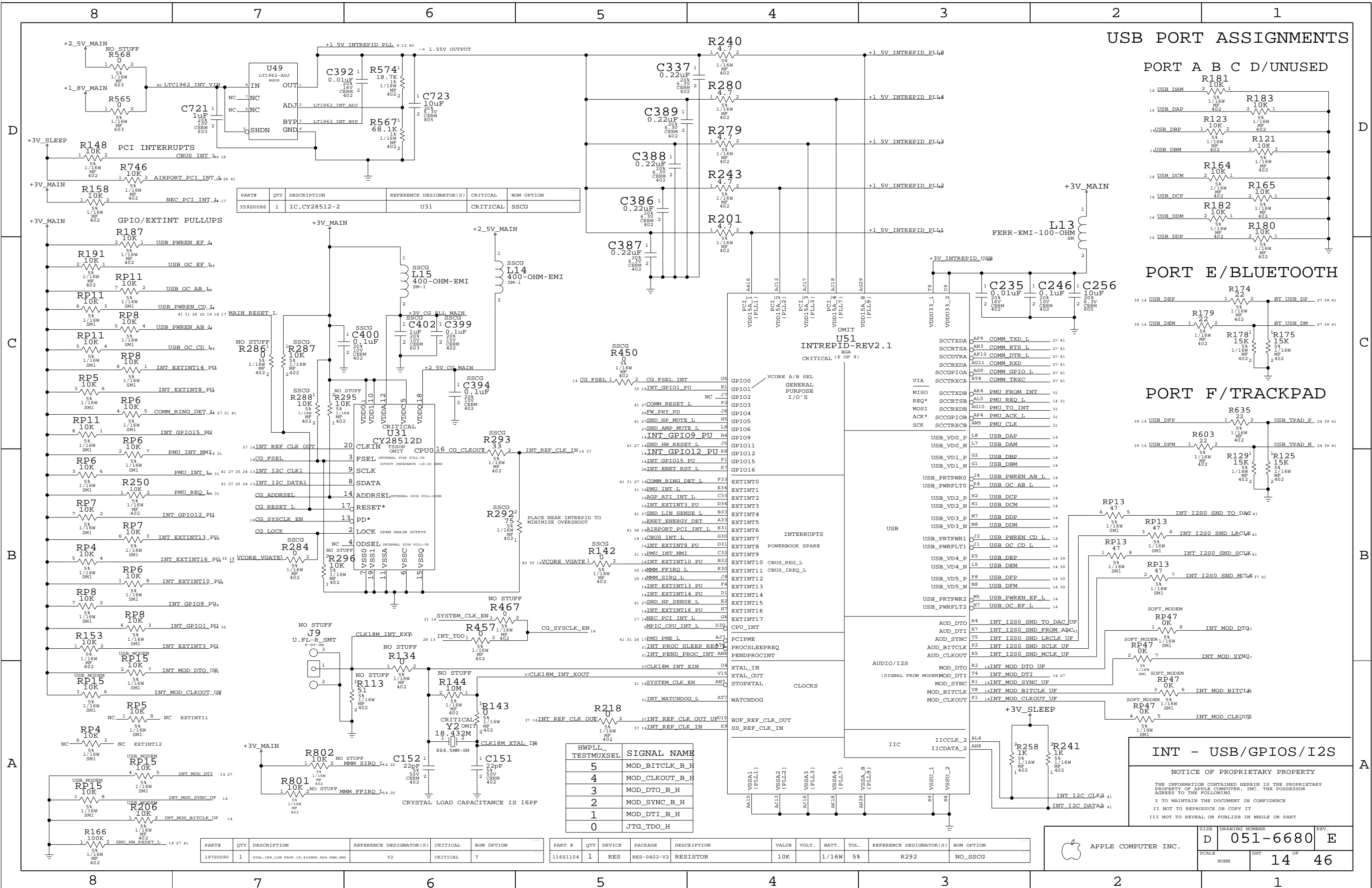
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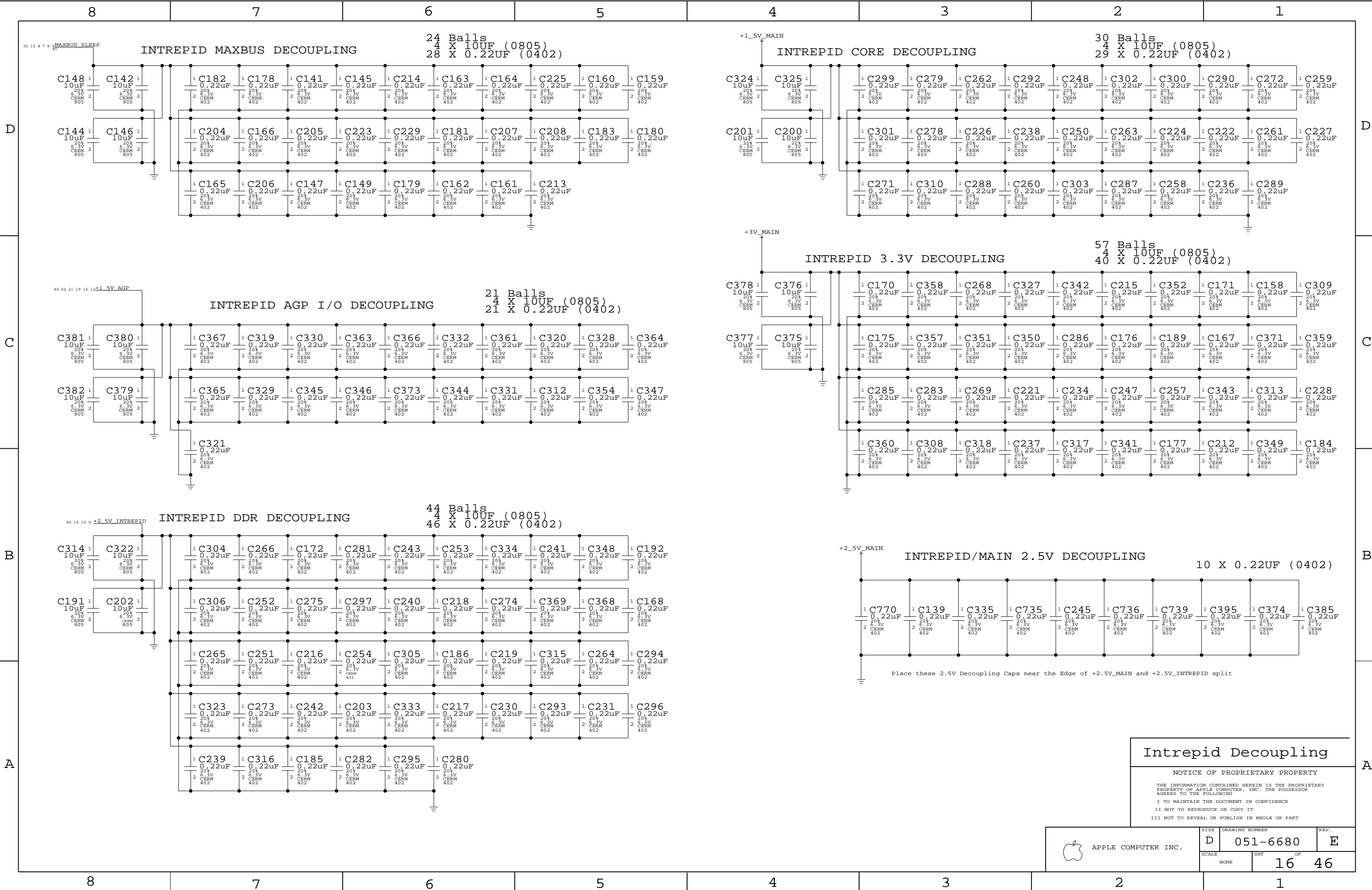
SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE	SHT	OF
NONE	14	46



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
19750090	1	XTAL, CER, LOW PROF, 18.432MHZ, 8X4, 5MM, SMD	Y2	CRITICAL	?

HWPLL TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG



Intrepid Decoupling

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SIZE

DRAWING NUMBER

D

051-6680

REV.

E

SCALE

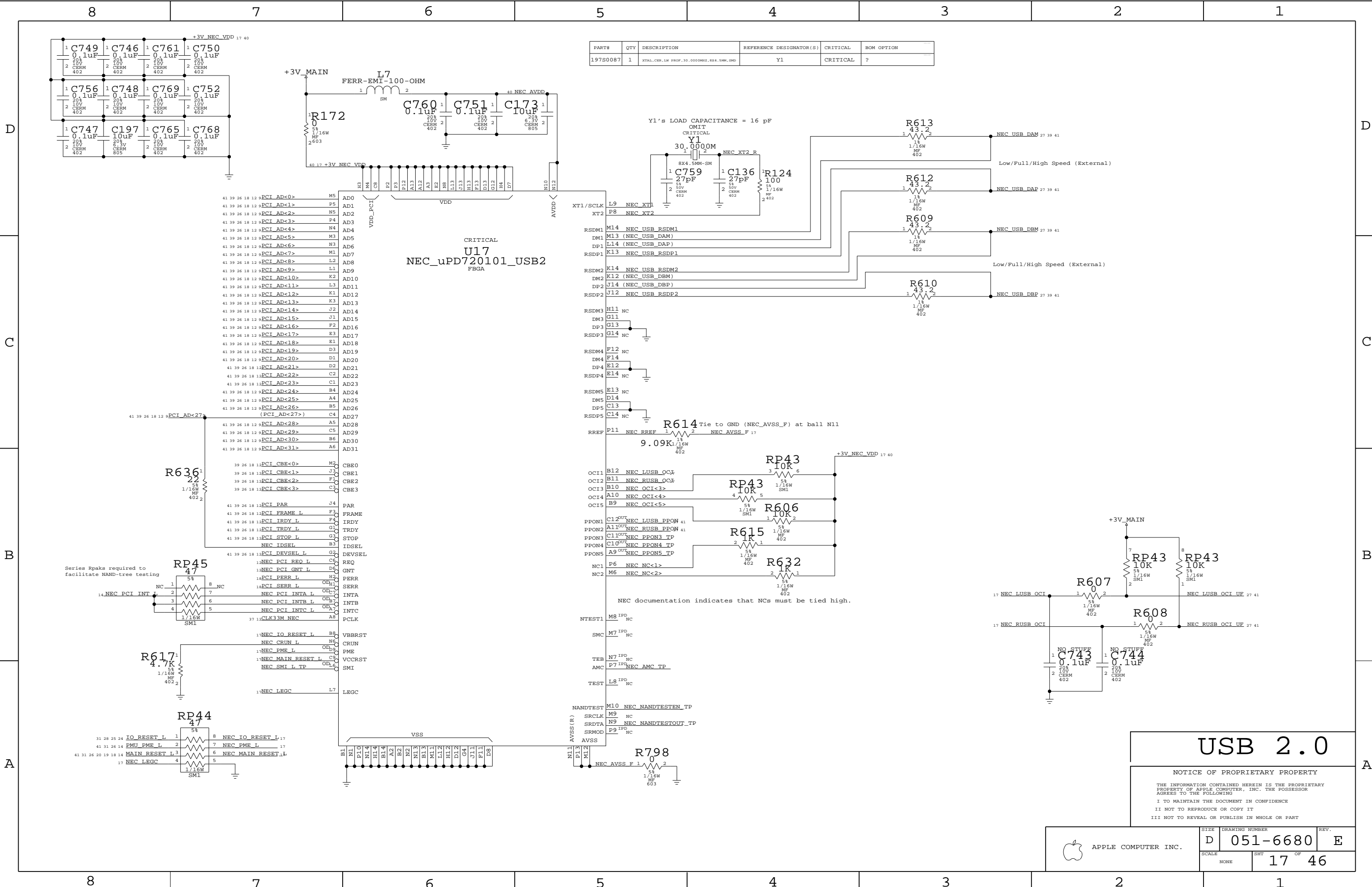
NONE

SHT

OF

16

46



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL, CER, 16 MHZ, 30.0000MHZ, 8X4.5MM, SMD	Y1	CRITICAL	?

USB 2.0

NOTICE OF PROPRIETARY PROPERTY

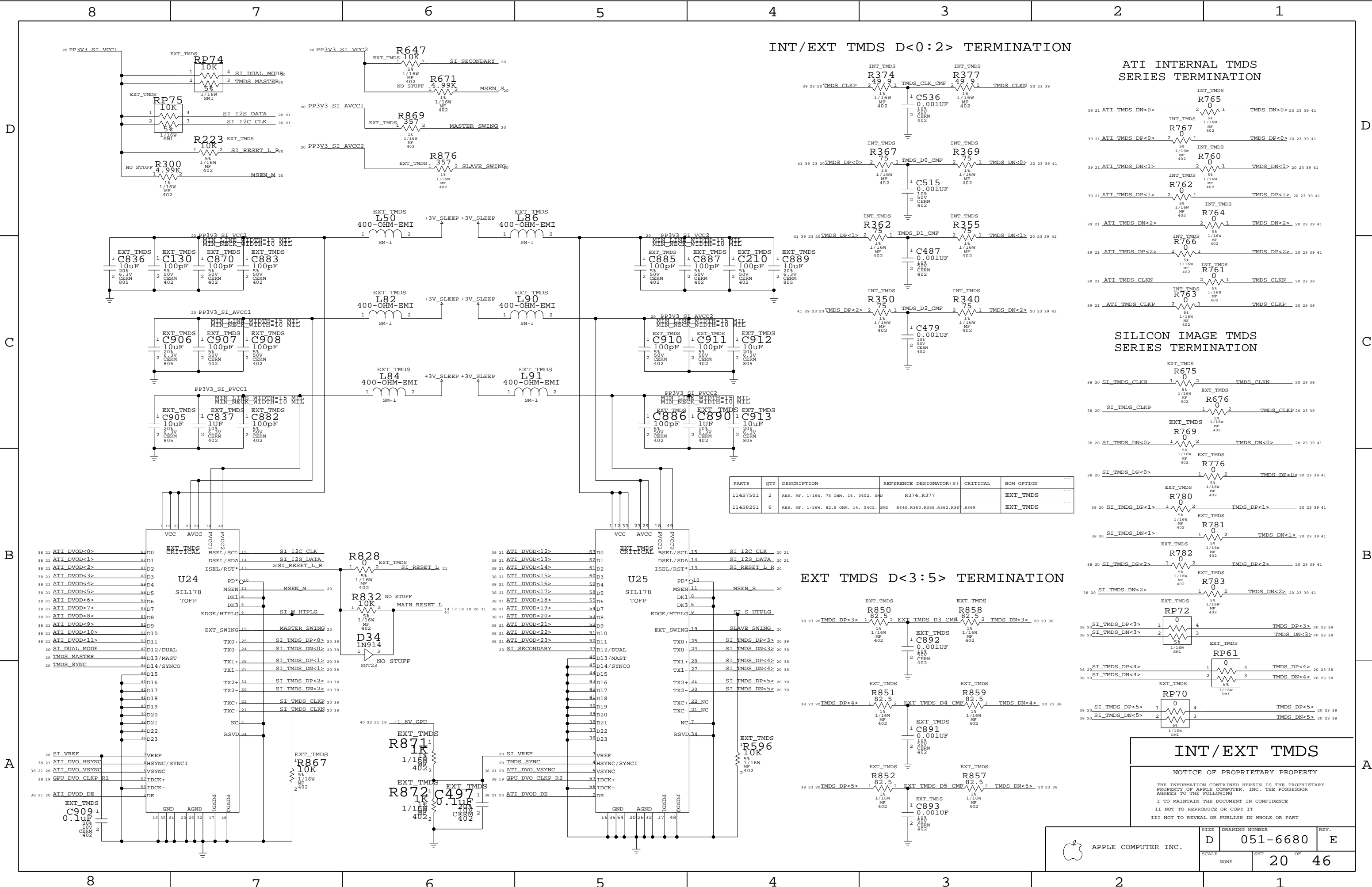
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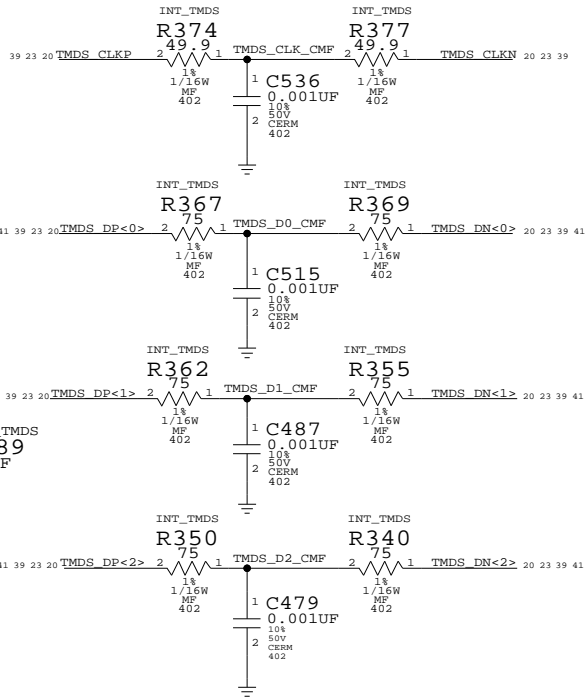
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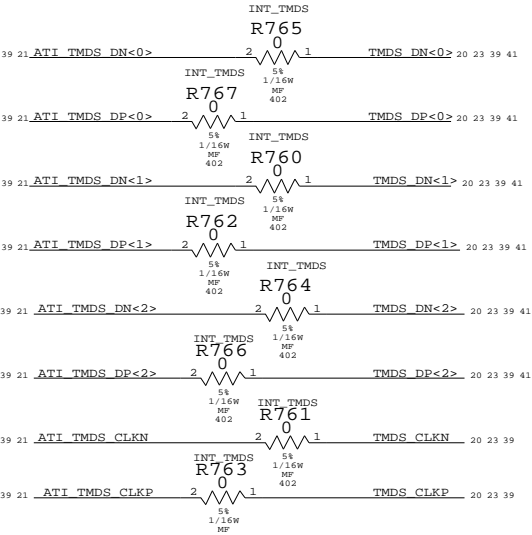
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6680	E
SCALE		SHT	OF
NONE		17	46



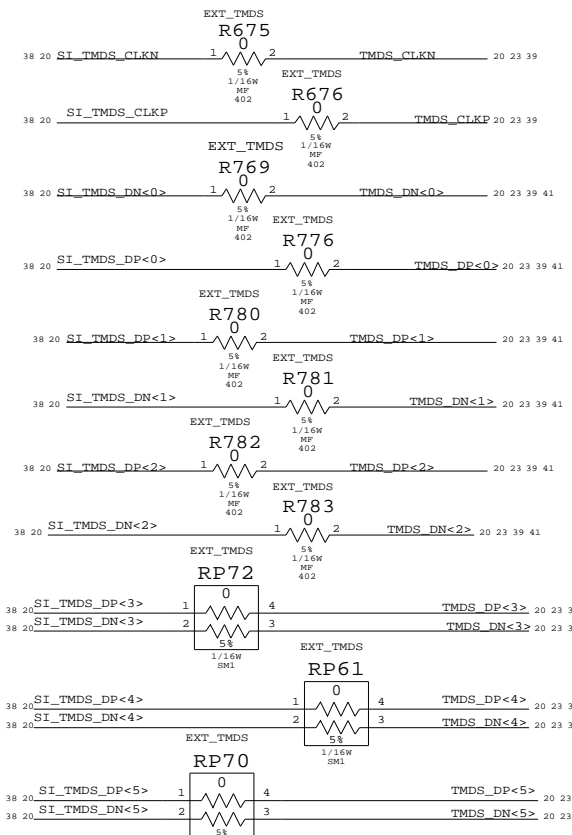
INT/EXT TMD5 D<0:2> TERMINATION



ATI INTERNAL TMD5 SERIES TERMINATION

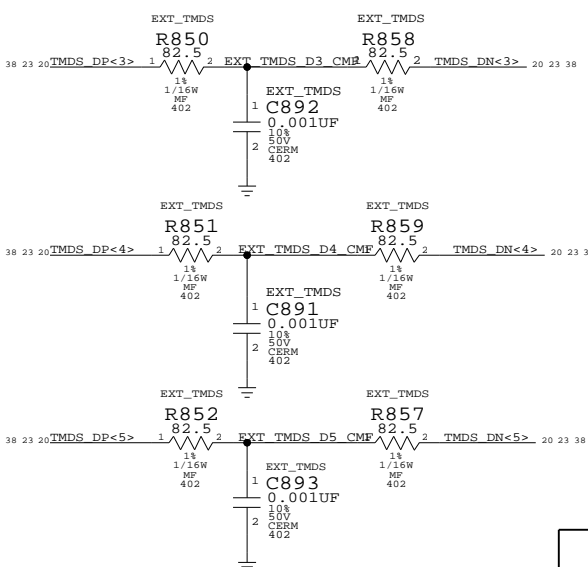


SILICON IMAGE TMD5 SERIES TERMINATION



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11487501	2	RES, MF, 1/16W, 75 OHM, 1%, 0402, SMD	R374, R377		EXT_TMD5
11488251	6	RES, MF, 1/16W, 82.5 OHM, 1%, 0402, SMD	R340, R350, R355, R362, R367, R369		EXT_TMD5

EXT TMD5 D<3:5> TERMINATION



INT/EXT TMD5

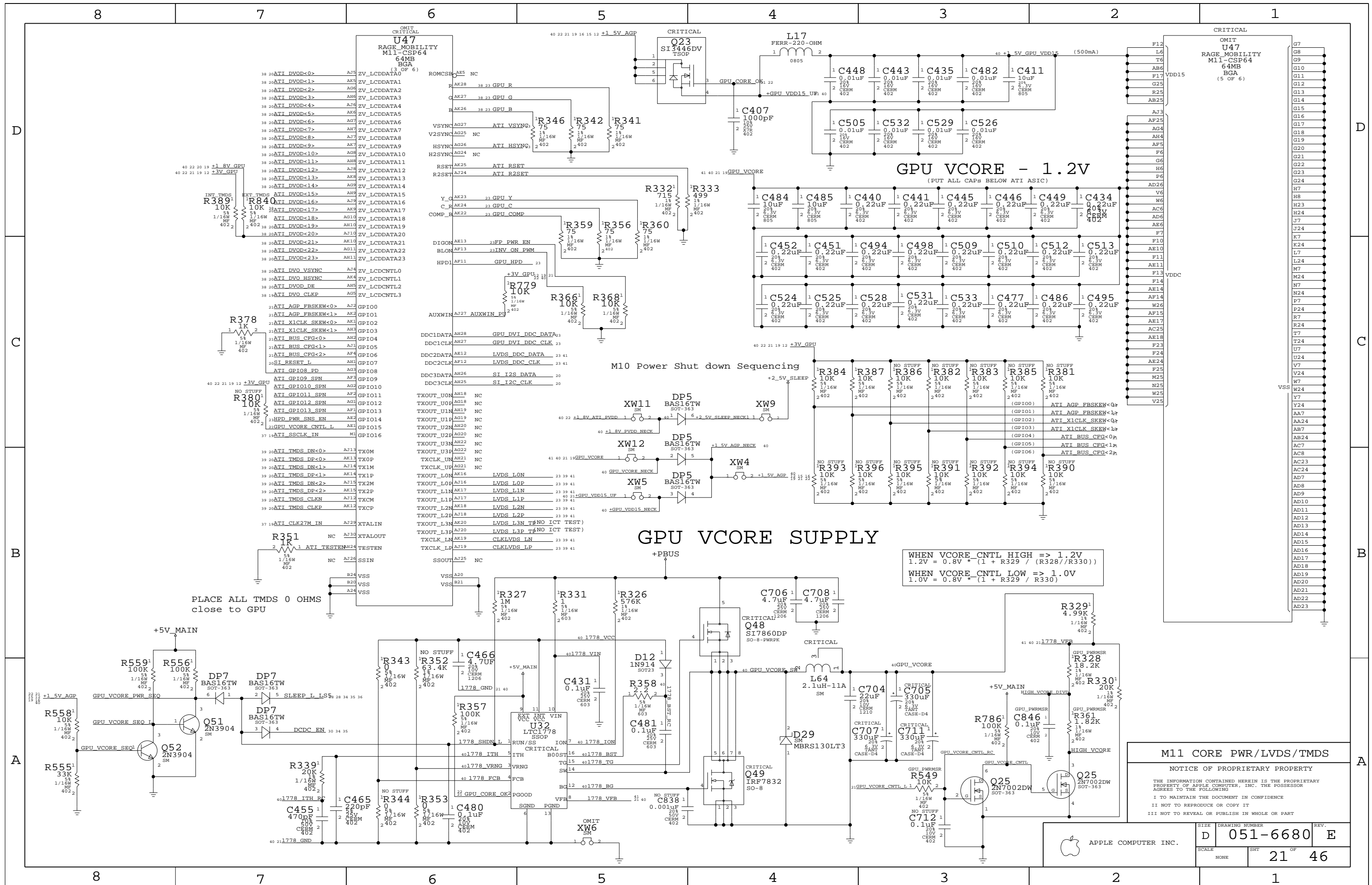
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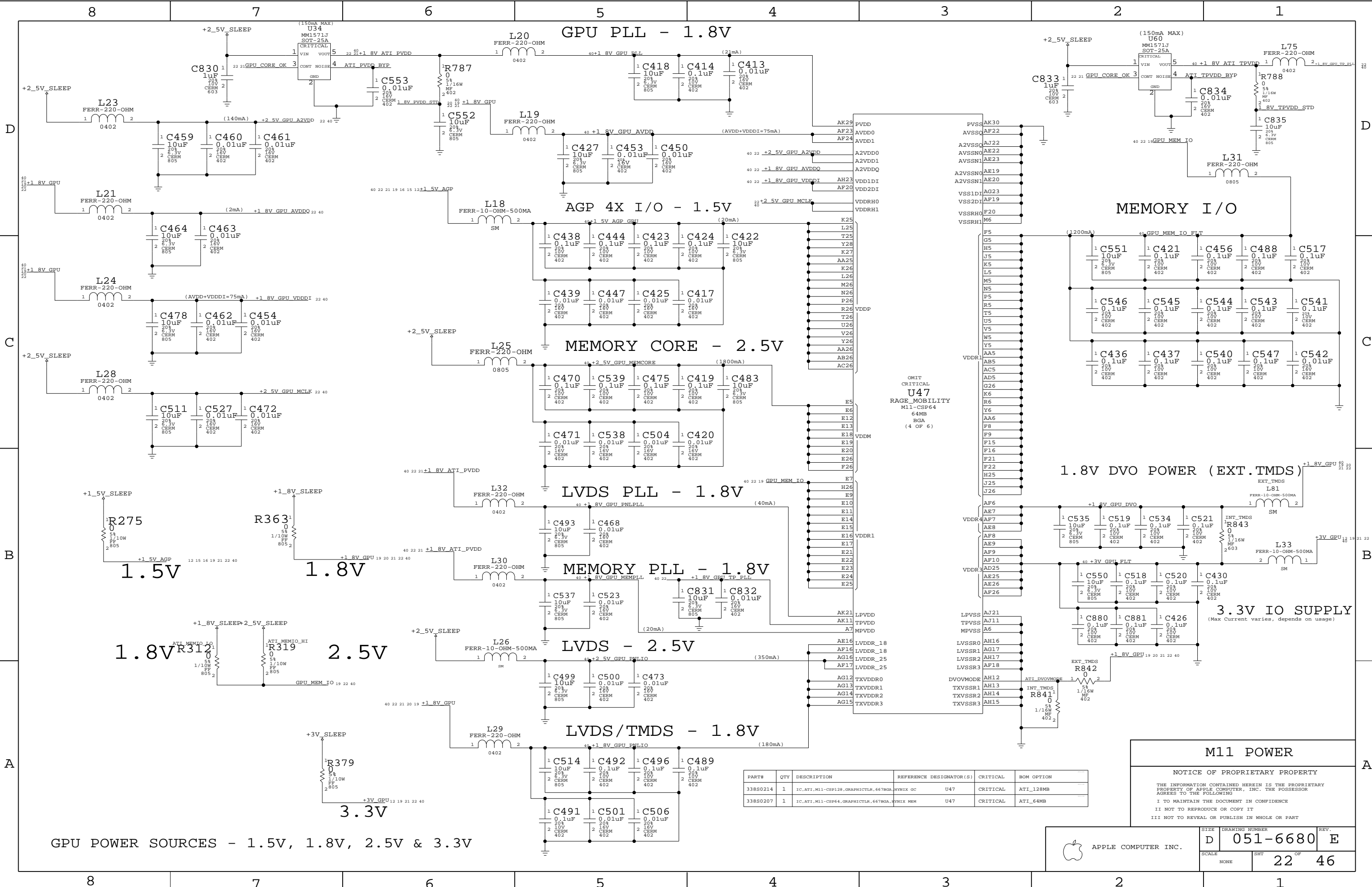
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SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE	SHT	OF
NONE	20	46





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0214	1	IC,ATI,M11-CS128,GRAPHICCTLR,667BGA,HYNIX GC	U47	CRITICAL	ATI_128MB
338S0207	1	IC,ATI,M11-CSP64,GRAPHICCTLR,667BGA,HYNIX MEM	U47	CRITICAL	ATI_64MB

M11 POWER

NOTICE OF PROPRIETARY PROPERTY

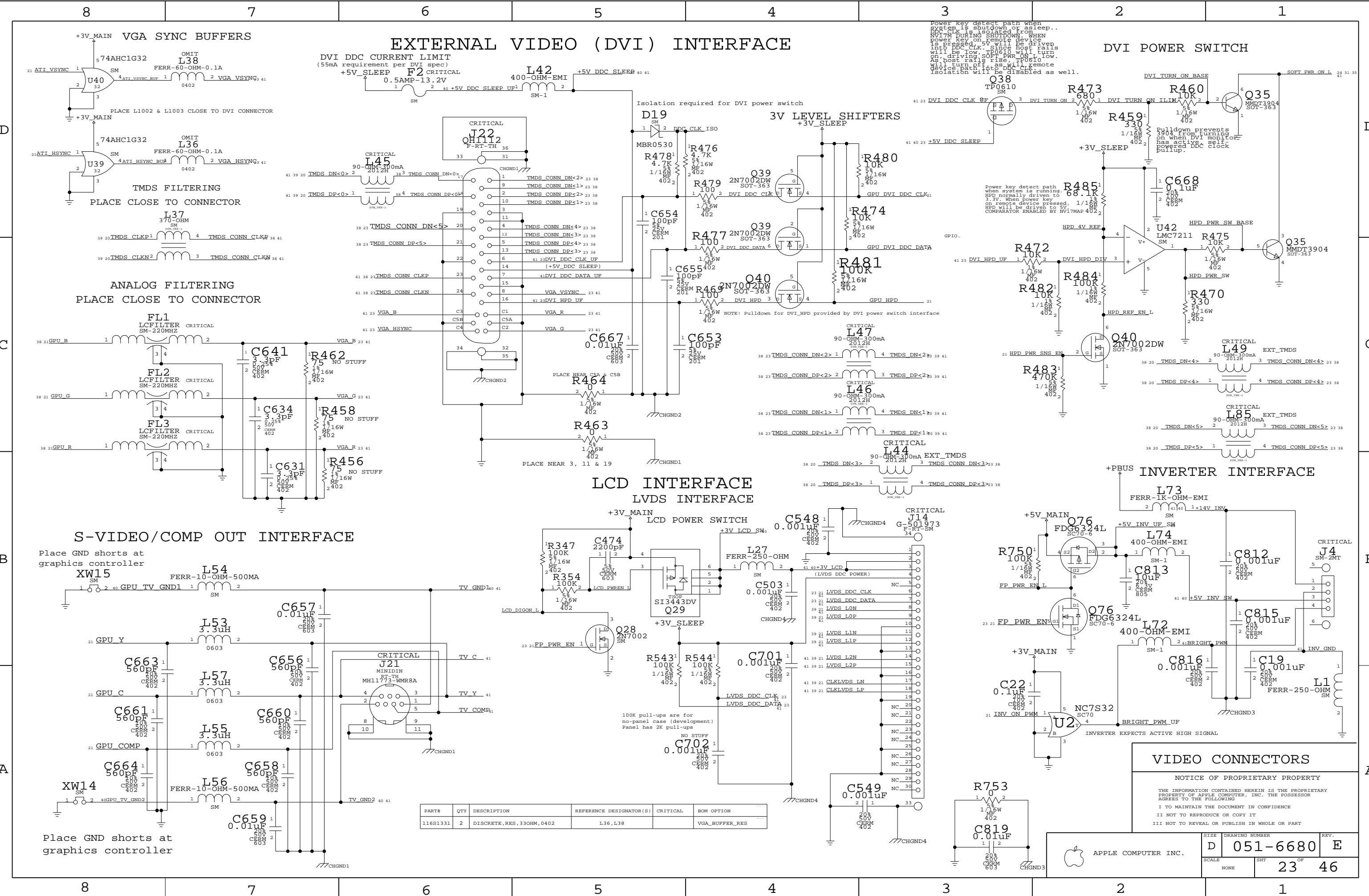
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SIZE	D	DRAWING NUMBER	051-6680	REV.	E
SCALE	NONE	SHT	22	OF	46



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE, RES, 330HM, 0402	L36, L38		VGA_BUFFER_RES

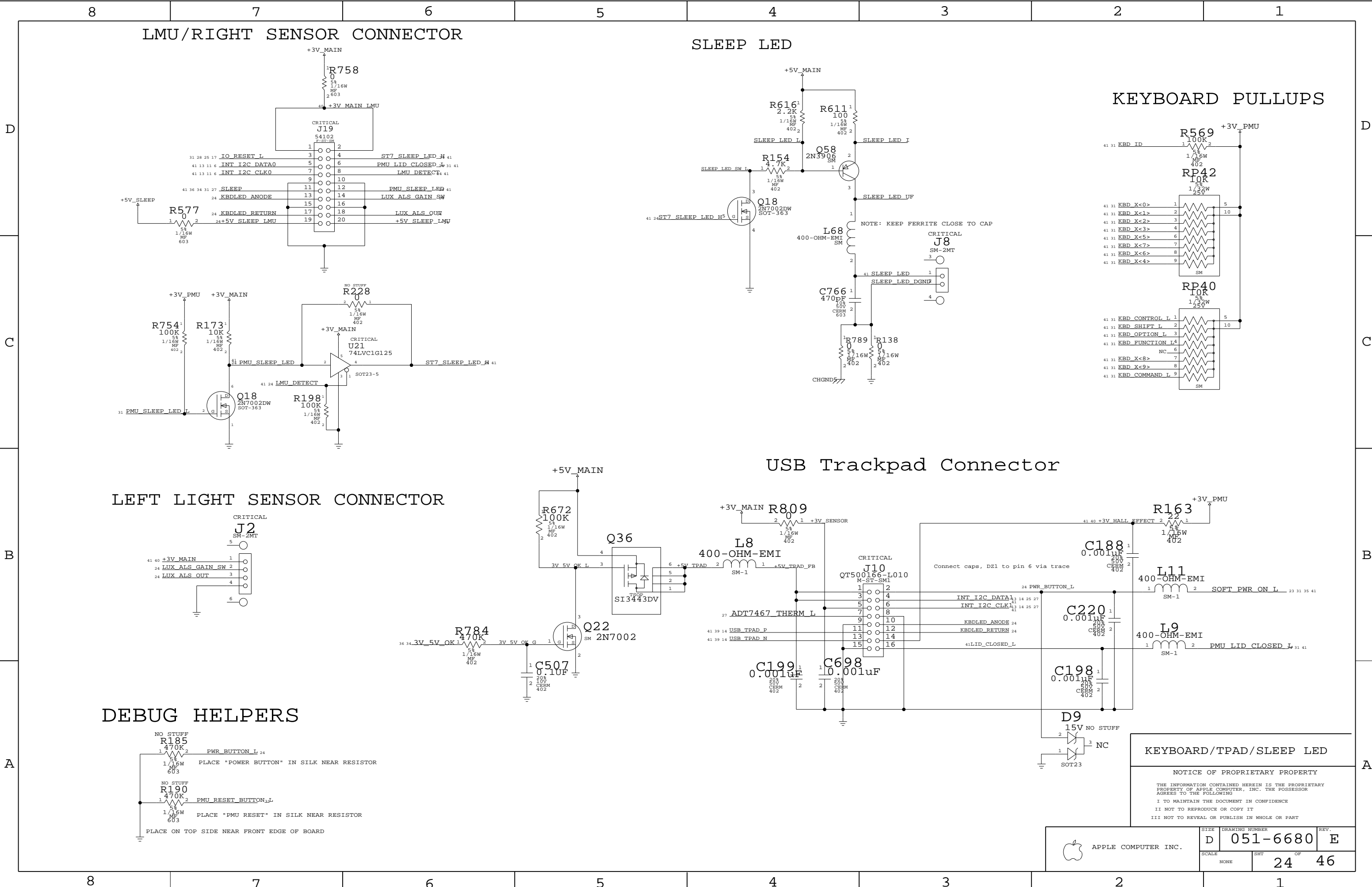
VIDEO CONNECTORS

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	D	051-6680	
NONE		SHT	23 OF 46



KEYBOARD/TPAD/SLEEP LED

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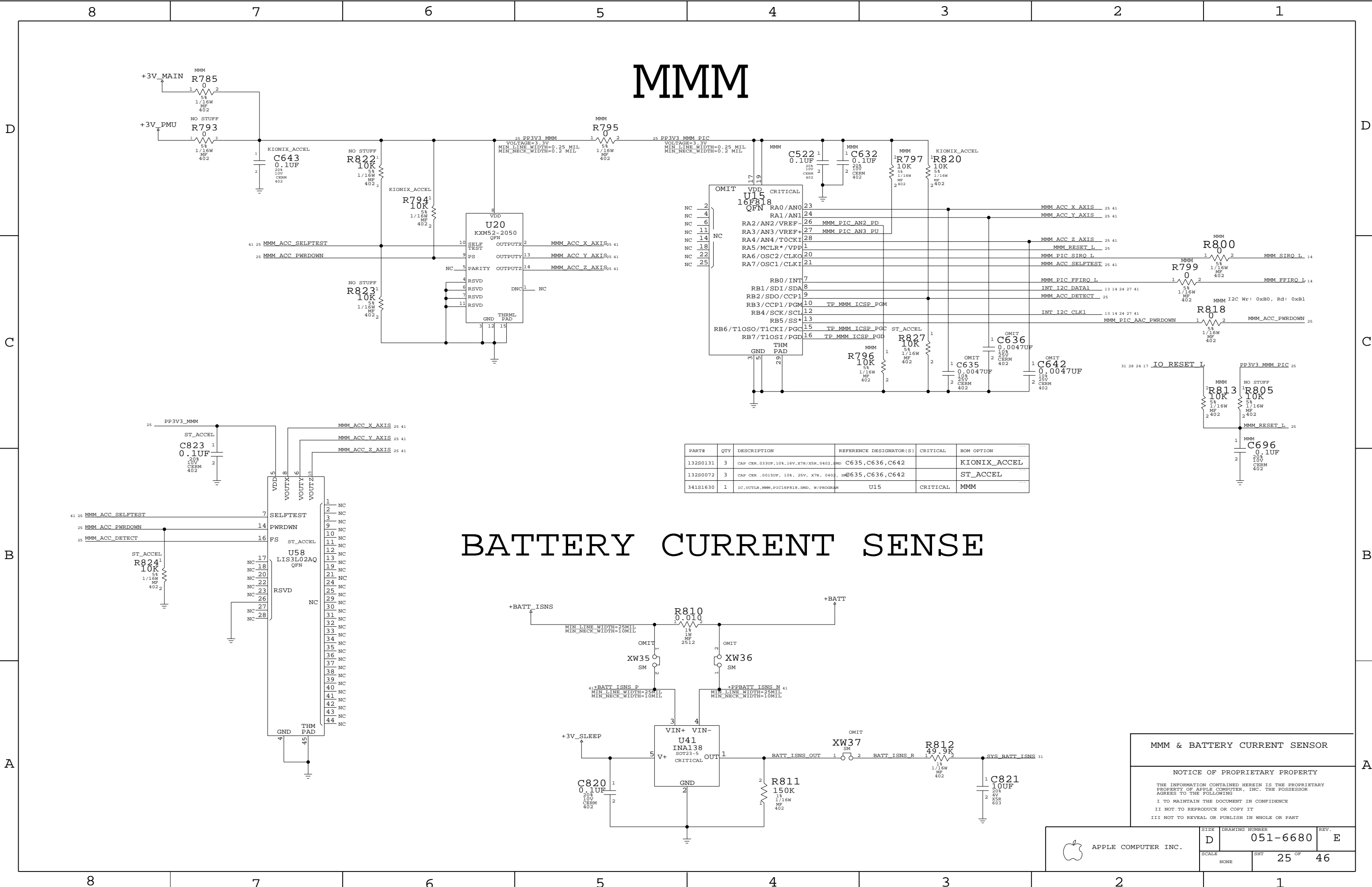


APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

D 051-6680 E

SCALE NONE SHT OF 24 46



MMM

BATTERY CURRENT SENSE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	CAP CER .03UF, 10%, 16V, X7R, 0402, SMD	C635, C636, C642		KIONIX_ACCEL
132S0072	3	CAP CER .0015UF, 10%, 25V, X7R, 0402, SMD	C635, C636, C642		ST_ACCEL
341S1630	1	IC, UCTLA, MMM, PIC16F818, SMD, W/PROGRAM	U15	CRITICAL	MMM

MMM & BATTERY CURRENT SENSOR

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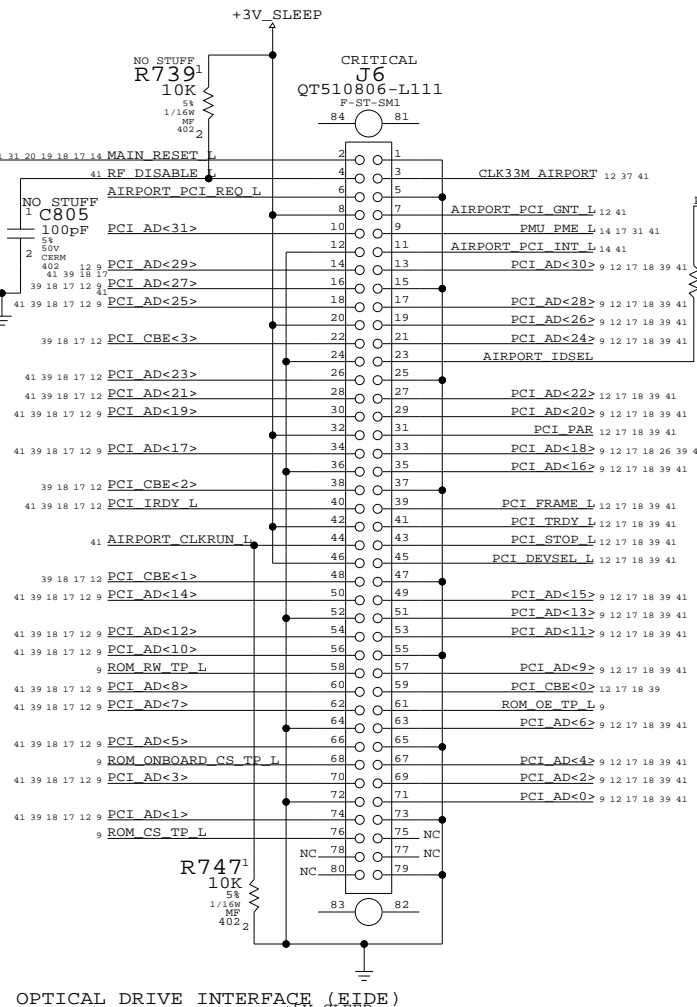
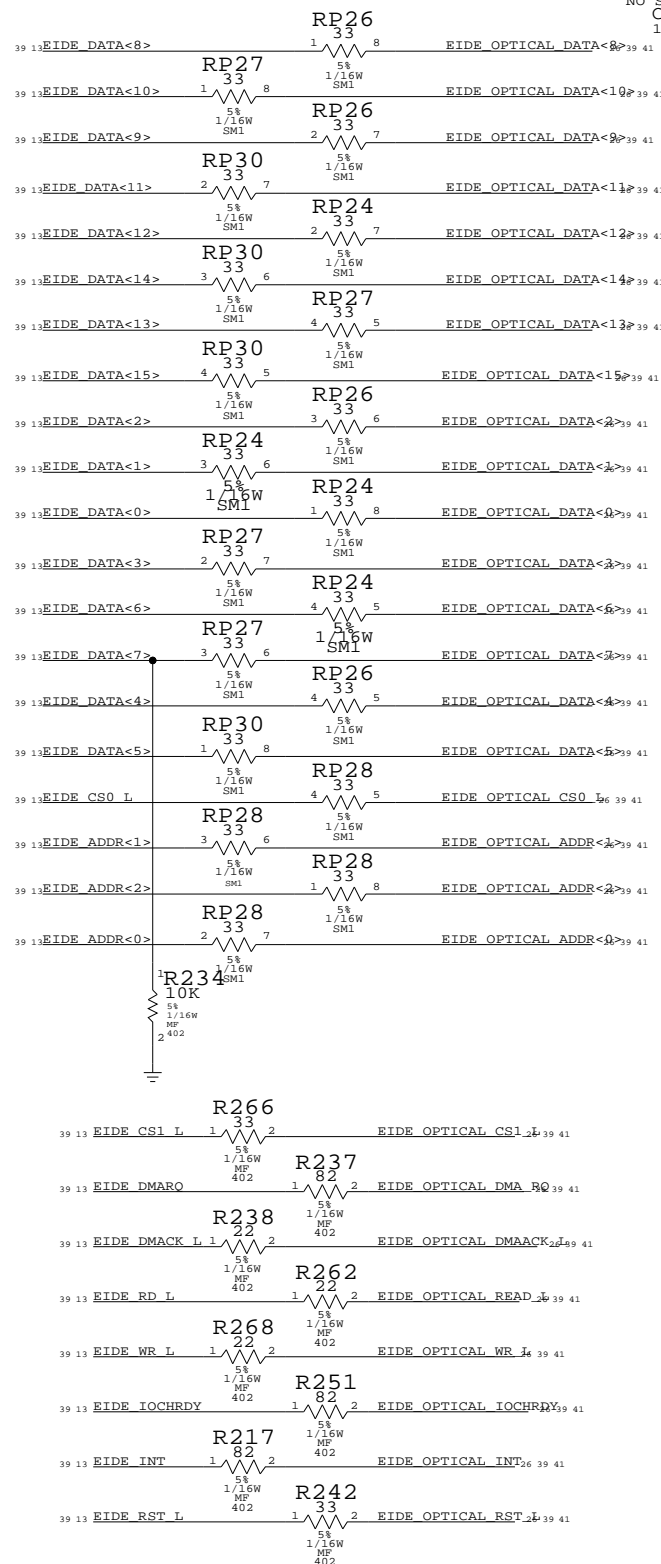
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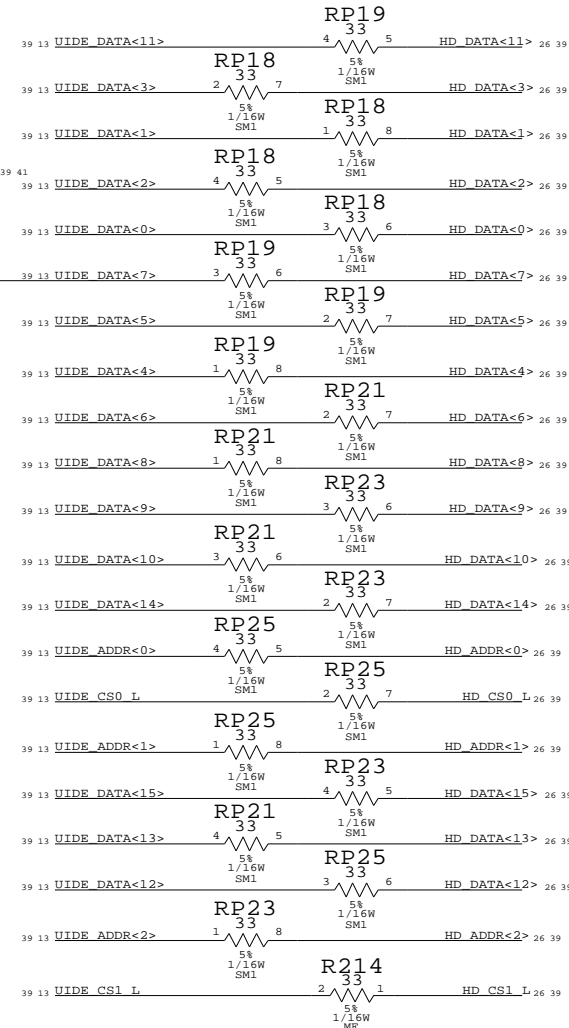
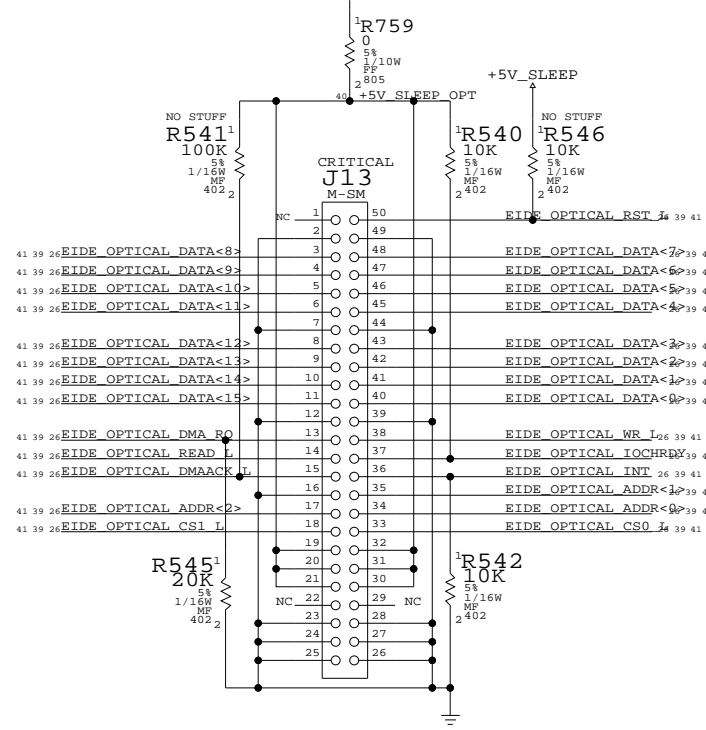
WIRELESS INTERFACE

HARD DRIVE INTERFACE (UATA100)

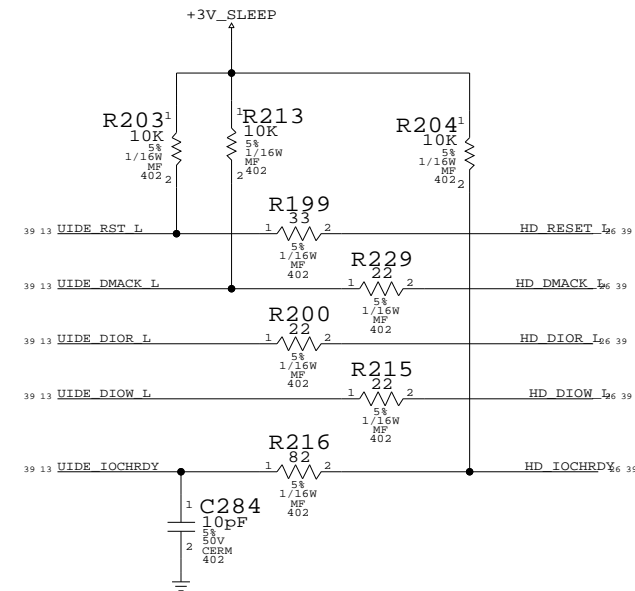
PLACE SERIES R CLOSE TO INTERPID



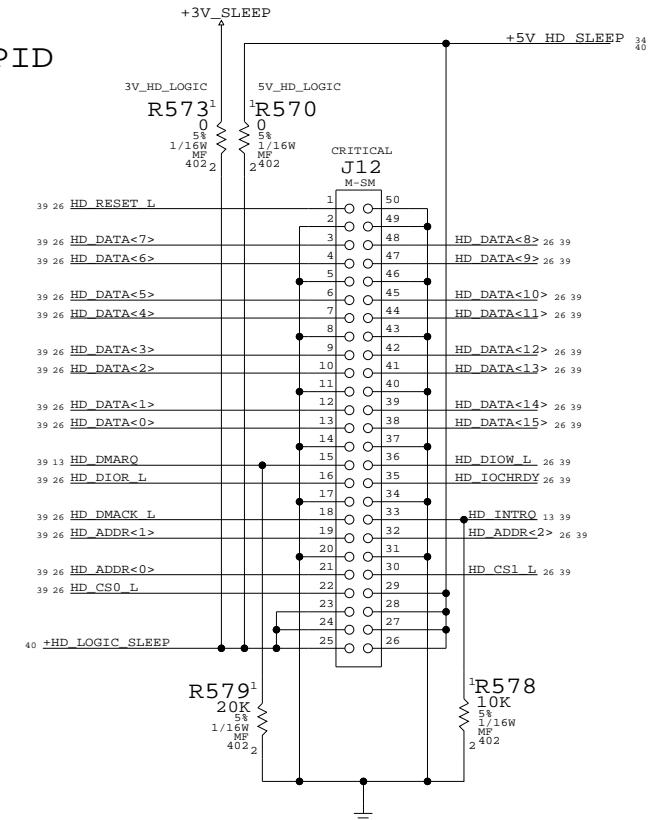
OPTICAL DRIVE INTERFACE (EIDE)



PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN
+5V_HD_SLEEP AND +3V_SLEEP

INTERNAL I/O CONNECTORS

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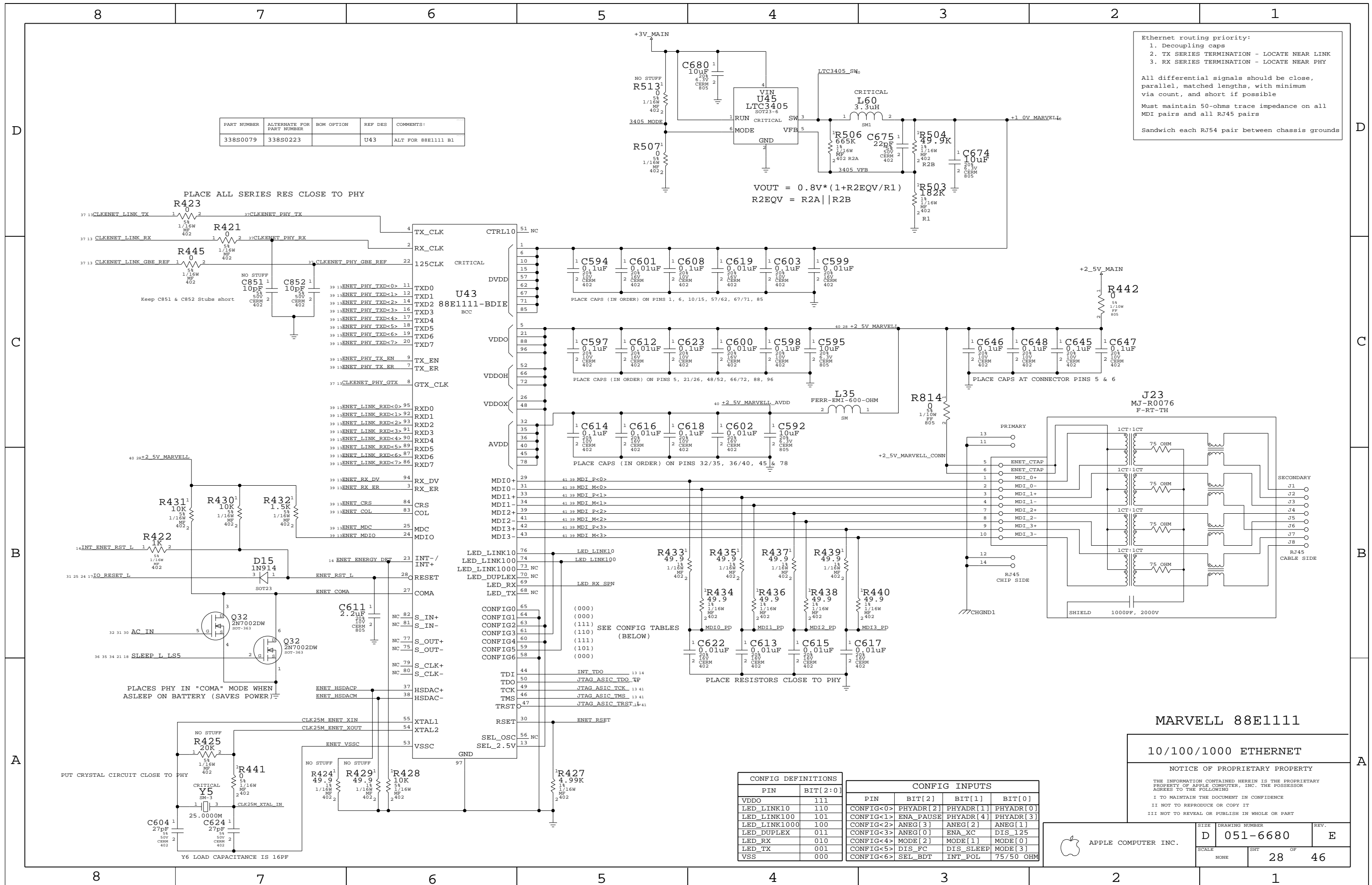


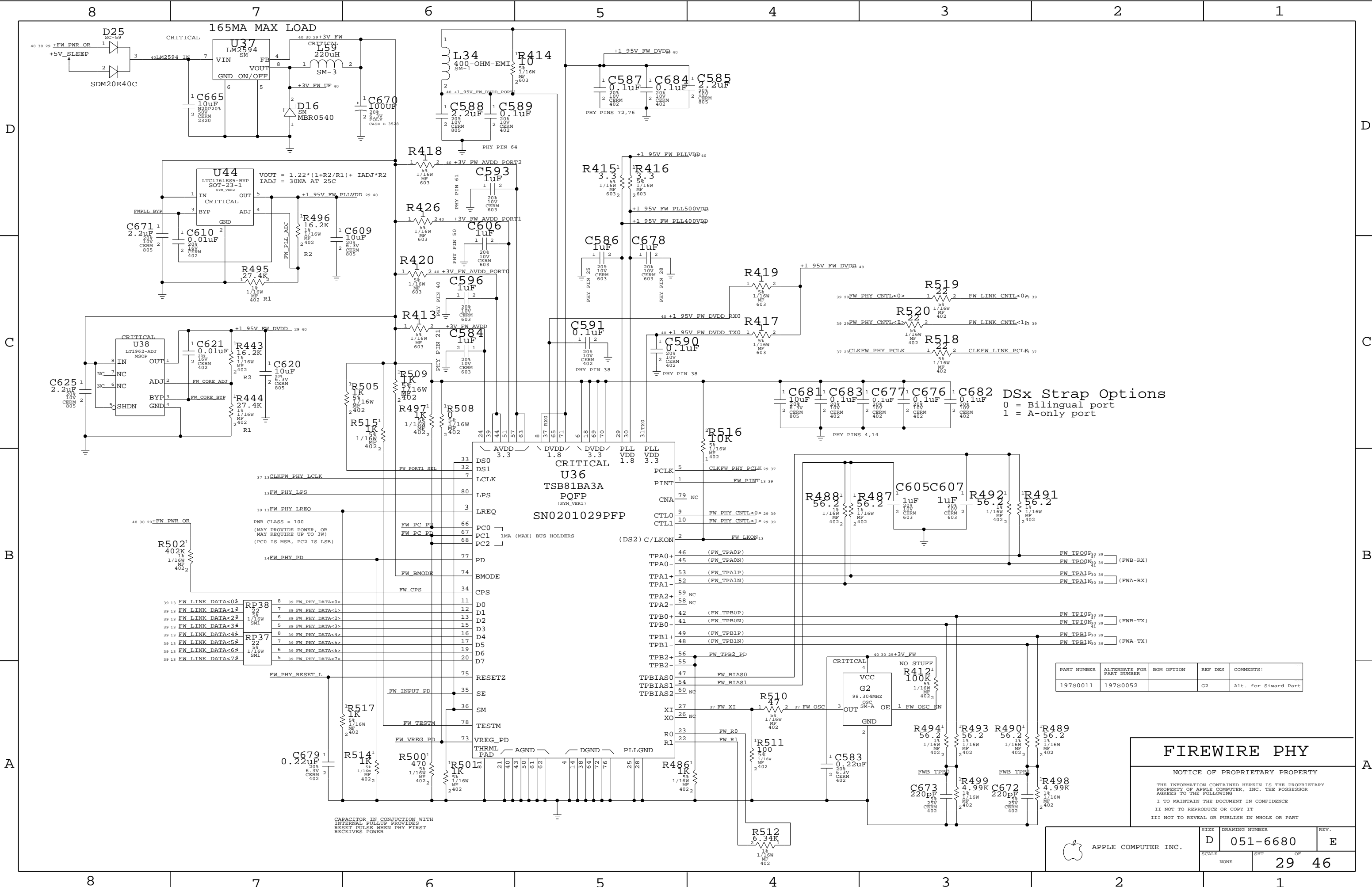
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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D	051-6680	E
---	----------	---

SCALE	SHT	OF
NONE	26	46





DSx Strap Options
0 = Bilingual port
1 = A-only port

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052		G2	Alt. for Siward Part

FIREWIRE PHY

NOTICE OF PROPRIETARY PROPERTY

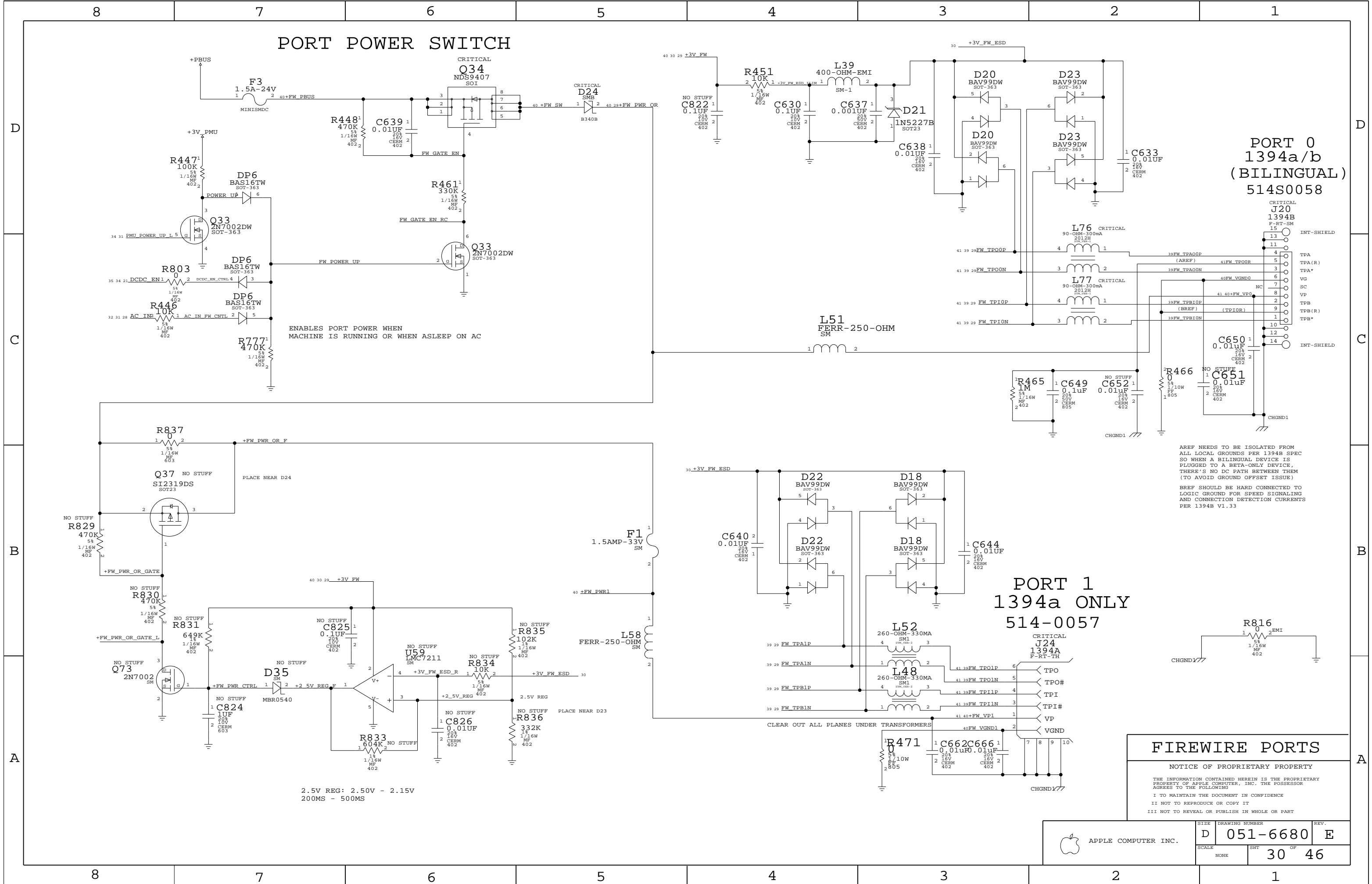
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PORT POWER SWITCH



FIREWIRE PORTS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE	SHT	OF
NONE	30	46

DC POWER INPUT

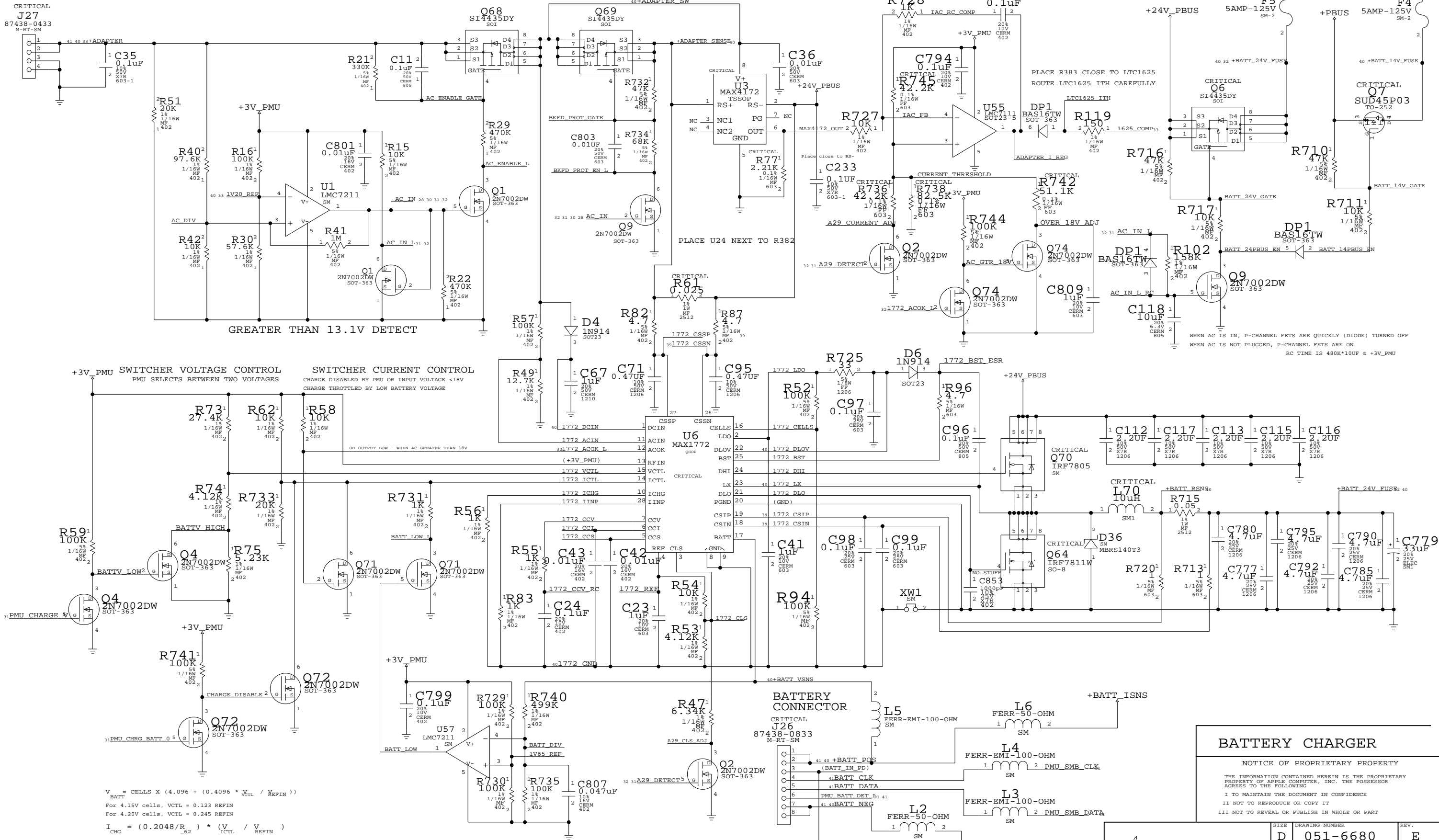
(POWER JACK, ETC. ON SEPARATE BOARD)

DC INRUSH LIMITER

BACKFEED PROTECTION

+PBUS CURRENT LIMIT

BATTERY SWITCH-OVER CIRCUIT



$$V_{BATT} = CELLS \times (4.096 + (0.4096 \times \frac{V_{VCTL}}{V_{REFIN}}))$$

For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN

$$I_{CHG} = (0.2048/R_{G2}) \times (\frac{V_{ICTL}}{V_{REFIN}})$$

BATTERY CHARGER

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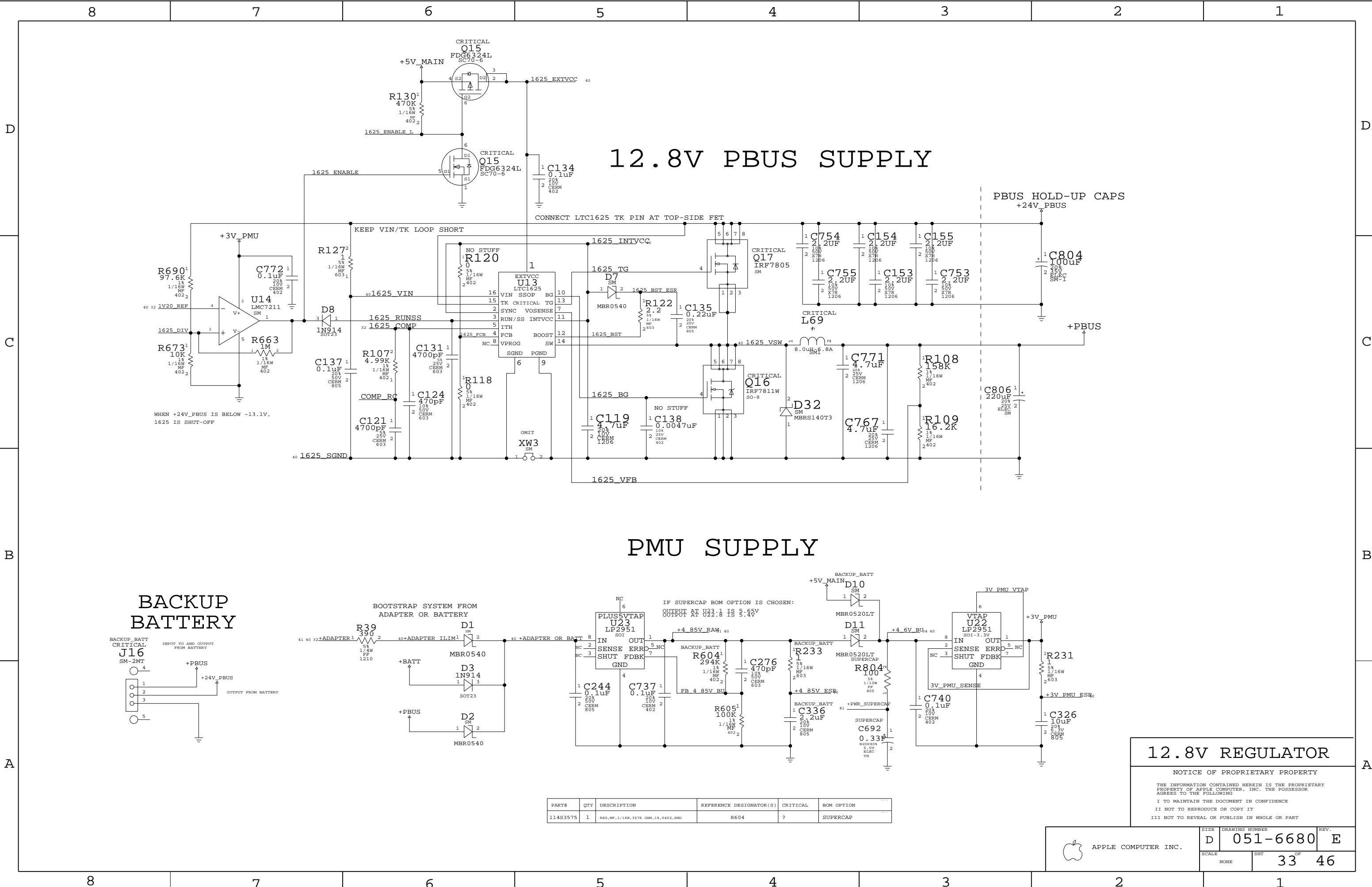
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE	SHT	OF
NONE	32	46



12.8V PBUS SUPPLY

PMU SUPPLY

BACKUP BATTERY

12.8V REGULATOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S3575	1	RES,MP,1/16W,357K OHM,1%,0402,SMD	R604	?	SUPERCAP


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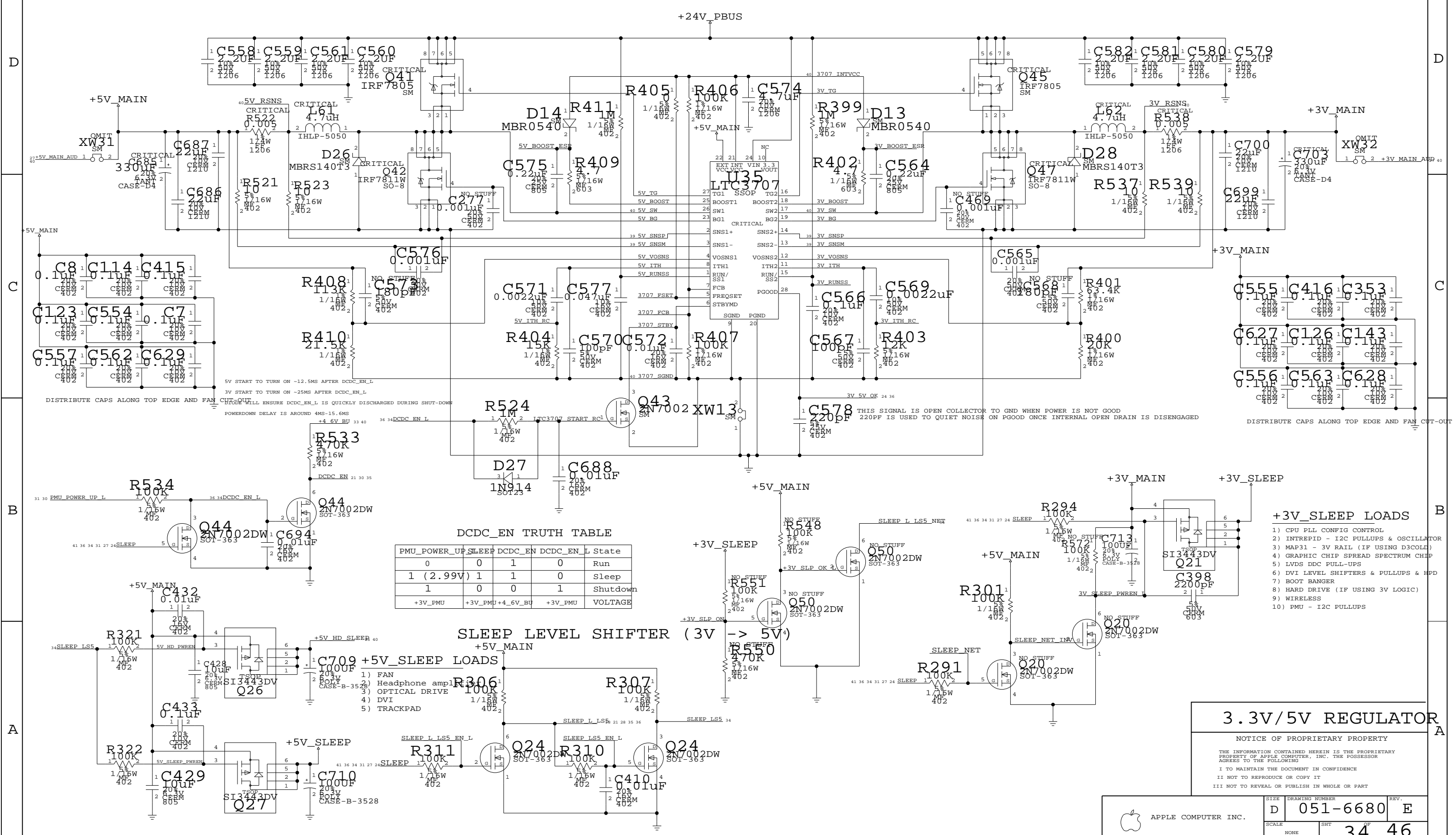
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 APPLE COMPUTER INC.

SIZE	D	DRAWING NUMBER	051-6680	REV.	E
SCALE	NONE	SHT	33	OF	46

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

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VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

+5V_MAIN

R101¹
100K
1/16W
MF
402 2

R106¹
100K
1/16W
MF
402 2

R111¹
100K
1/16W
MF
402 2

1.300V->0.975V

1.50GHZ 1.200V->0.975V

1.67GHZ 1.300V->0.975V

(VALUE WITHOUT OFFSET)

DP2 BAS16TW
SOT-363

Q8 2N3904

Q5 2N3904

DP2 BAS16TW
SOT-363

DP2 BAS16TW
SOT-363

SLEEP L LS55

DCDC EN

NO STUFF R80

R81

INT GPIO1_PU

+3V_MAIN

CPU_BTR

R66

<D0>

VCORE_VID<0>

VCORE_VID<1>

VCORE_VID<2>

VCORE_VID<3>

VCORE_VID<4>

CPU_BST&CPU_BST_VCORE126

R65

C66

R67

R95

C94

C80

VCORE_GND4

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DIGITAL SIGNALS	CLOCK LINE CONSTRAINTS							
	GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE_PARAM
	GROUP 0	MEM DATA<7..0>	L:S:1602:1700	7	500	(200)		167 MHZ
		MEM DOM<0>	L:S:1602 MTL:1700	MTL:7	500.0000	(200)		167.0 MHz
		MEM DOS<0>	L:S:1602 MTL:1700	MTL:7	500.0000	(200)		167.0 MHz
		RAM DATA A<7..0>	L:S:1903:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET	167 MHZ
		RAM DOM A<0>	L:S:1903 MTL:2000	MTL:7	500.0000	(200)		167.0 MHz
		RAM DOS A<0>	L:S:1903 MTL:2000	MTL:7	500.0000	(200)		167.0 MHz
		RAM DATA B<7..0>	L:S:2000:2100	7	500	(200)		167 MHZ
		RAM DOM B<0>	L:S:2000 MTL:2100	MTL:7	500.0000	(200)		167.0 MHz
		RAM DOS B<0>	L:S:2000 MTL:2100	MTL:7	500.0000	(200)		167.0 MHz
	GROUP 1	MEM DATA<15..8>	L:S:1344:1660	7	500	(200)		167 MHZ
		MEM DOM<1>	L:S:1344 MTL:1660	MTL:7	500.0000	(200)		167.0 MHz
		MEM DOS<1>	L:S:1344 MTL:1660	MTL:7	500.0000	(200)		167.0 MHz
		RAM DATA A<15..8>	L:S:1905:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET	167 MHZ
		RAM DOM A<1>	L:S:1905 MTL:2000	MTL:7	500.0000	(200)		167.0 MHz
		RAM DOS A<1>	L:S:1905 MTL:2000	MTL:7	500.0000	(200)		167.0 MHz
		RAM DATA B<15..8>	L:S:2004:2412	7	500	(200)		167 MHZ
		RAM DOM B<1>	L:S:2004 MTL:2412	MTL:7	500.0000	(200)		167.0 MHz
		RAM DOS B<1>	L:S:2004 MTL:2412	MTL:7	500.0000	(200)		167.0 MHz
	GROUP 2	MEM DATA<23..16>	L:S:1435:1500	7	500	(200)		167 MHZ
		MEM DOM<2>	L:S:1435 MTL:1500	MTL:7	500.0000	(200)		167.0 MHz
		MEM DOS<2>	L:S:1435 MTL:1500	MTL:7	500.0000	(200)		167.0 MHz
		RAM DATA A<23..16>	L:S:1707:1800	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET	167 MHZ
		RAM DOM A<2>	L:S:1707 MTL:1800	MTL:7	500.0000	(200)		167.0 MHz
		RAM DOS A<2>	L:S:1707 MTL:1800	MTL:7	500.0000	(200)		167.0 MHz
		RAM DATA B<23..16>	L:S:1900:2000	7	500	(200)		167 MHZ
		RAM DOM B<2>	L:S:1900 MTL:2000	MTL:7	500.0000	(200)		167.0 MHz
		RAM DOS B<2>	L:S:1900 MTL:2000	MTL:7	500.0000	(200)		167.0 MHz
	GROUP 3	MEM DATA<31..24>	L:S:1233:1485	7	500	(200)		167 MHZ
		MEM DOM<3>	L:S:1233 MTL:1485	MTL:7	500.0000	(200)		167.0 MHz
		MEM DOS<3>	L:S:1233 MTL:1485	MTL:7	500.0000	(200)		167.0 MHz
		RAM DATA A<31..24>	L:S:1700:2165	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET	167 MHZ
		RAM DOM A<3>	L:S:1700 MTL:2165	MTL:7	500.0000	(200)		167.0 MHz
		RAM DOS A<3>	L:S:1700 MTL:2165	MTL:7	500.0000	(200)		167.0 MHz
		RAM DATA B<25..24>	L:S:1907:2356	7	500	(200)		167 MHZ
		RAM DATA B<26>	L:S:1907 MTL:2356	MTL:7	500.0000	(200)		167.0 MHz
		RAM DATA B<31..27>	L:S:1907:2356	7	500	(200)		167 MHZ
		RAM DOM B<3>	L:S:1907 MTL:2356	MTL:7	500.0000	(200)		167.0 MHz
		RAM DOS B<3>	L:S:1907 MTL:2356	MTL:7	500.0000	(200)		167.0 MHz
	GROUP 4	MEM DATA<39..32>	L:S:1915:2000	7	500	(200)		167 MHZ
		MEM DOM<4>	L:S:1915 MTL:2000	MTL:7	500.0000	(200)		167.0 MHz
		MEM DOS<4>	L:S:1915 MTL:2000	MTL:7	500.0000	(200)		167.0 MHz
		RAM DATA A<39..32>	L:S:1205:1387	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET	167 MHZ
		RAM DOM A<4>	L:S:1205 MTL:1387	MTL:7	500.0000	(200)		167.0 MHz
		RAM DOS A<4>	L:S:1205 MTL:1387	MTL:7	500.0000	(200)		1

8		7		6		5		4		3		2		1		
DIGITAL SIGNALS	MAXBUS	GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIA	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PRO_TEST	PULSE_PARAMS						
			CPU_AACK_L	L:S:1500 MIL:2700	MIL ₇		(250)									
			CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ						
			CPU_ARTRY_L	L:S:1500 MIL:2700	MIL ₇		(250)									
			CPU_BG_L	L:S:1500 MIL:2700	MIL ₇		(250)									
			CPU_BR_L	L:S:1500 MIL:2700	MIL ₇		(250)									
			CPU_CI_L	L:S:1500 MIL:2700	MIL ₇		(250)									
			CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ						
			CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ						
			CPU_DBG_L	L:S:1500 MIL:2700	MIL ₇		(250)									
			CPU_DTI<0..2>	L:S:1500:2950	7		(250)									
			CPU_DRDY_L	L:S:1500 MIL:3200	MIL ₇		(250)									
			CPU_GBL_L	L:S:1500 MIL:2700	MIL ₇		(250)									
			CPU_HIT_L	L:S:1500 MIL:2800	MIL ₇		(250)									
			CPU_QACK_L	L:S:1500 MIL:2700	MIL ₇		(250)									
			CPU_OREQ_L	L:S:1500 MIL:2700	MIL ₇		(250)									
			CPU_TA_L	L:S:1500 MIL:2700	MIL ₇		(250)									
			CPU_TBST_L	L:S:1500 MIL:2700	MIL ₇		(250)									
			CPU_TEA_L	L:S:1500 MIL:3000	MIL ₇		(250)									
			CPU_TS_L	L:S:1500 MIL:2700	MIL ₇		(250)									
			CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)									
			CPU_TT<0..4>	L:S:1500:3400	7		(250)									
			CPU_WT_L	L:S:1500 MIL:3100	MIL ₇		(250)									

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POWER NET CONSTRAINTS																																																																																																																																																																																																																																																																																																																										
GROUP					SIG_NAME					VOLTAGE					MIN_LINE_WIDTH					MIN_NECK_WIDTH					GROUP					SIG_NAME					VOLTAGE					MIN_LINE_WIDTH					MIN_NECK_WIDTH																																																																																																																																																																																																																																																																													
D	MAIN/SLEEP				+24V PBUS			VOLTAGE=24V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41			CPU				CPU_VCORE_SLEEP			VOLTAGE=1.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			5 6 35 41																																																																																																																																																																																																																																																																																						
					+BATT			VOLTAGE=12.8V			MIN_LINE_WIDTH=10			MIN_NECK_WIDTH=25			MIL							CPU_AVDD			VOLTAGE=1.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			5																																																																																																																																																																																																																																																																																						
					+PBUS			VOLTAGE=12.8V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41							MAXBUS_SLEEP			VOLTAGE=1.8V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			5 6 7 8 15 16 35																																																																																																																																																																																																																																																																																						
					+5V MAIN			VOLTAGE=5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41							CPU_AVDD_VIN			VOLTAGE=3.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			5																																																																																																																																																																																																																																																																																						
					+5V_SLEEP			VOLTAGE=5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41							CPU_AVDD_VOUT			VOLTAGE=1.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			5																																																																																																																																																																																																																																																																																						
					+3V MAIN			VOLTAGE=3.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			24 41							DDR_VREF			VOLTAGE=1.25V			MIN_LINE_WIDTH=10			11																																																																																																																																																																																																																																																																																									
					+3V_SLEEP			VOLTAGE=3.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=6			41							INTREPID			VOLTAGE=2.5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			9 10 15 16																																																																																																																																																																																																																																																																																						
					+3V_PMU			VOLTAGE=3.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41							INTREPID_USB			VOLTAGE=3.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			14																																																																																																																																																																																																																																																																																						
					+2.5V MAIN			VOLTAGE=2.5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41							+1.5V INTREPID PLL			VOLTAGE=1.5V			MIN_LINE_WIDTH=15			MIN_NECK_WIDTH=10			8 12 14																																																																																																																																																																																																																																																																																						
					+2.5V_SLEEP			VOLTAGE=2.5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41							+1.5V INTREPID PLL1			VOLTAGE=1.5V			MIN_LINE_WIDTH=15			MIN_NECK_WIDTH=6			14																																																																																																																																																																																																																																																																																						
					+1.8V MAIN			VOLTAGE=1.8V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=6			41							+1.5V INTREPID PLL2			VOLTAGE=1.5V			MIN_LINE_WIDTH=15			MIN_NECK_WIDTH=6			14																																																																																																																																																																																																																																																																																						
					+1.8V_SLEEP			VOLTAGE=1.8V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41							+1.5V INTREPID PLL3			VOLTAGE=1.5V			MIN_LINE_WIDTH=10			MIN_NECK_WIDTH=6			14																																																																																																																																																																																																																																																																																						
					+1.5V MAIN			VOLTAGE=1.5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41							+1.5V INTREPID PLL4			VOLTAGE=1.5V			MIN_LINE_WIDTH=10			MIN_NECK_WIDTH=6			14																																																																																																																																																																																																																																																																																						
					+1.5V_SLEEP			VOLTAGE=1.5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41							+1.5V INTREPID PLL5			VOLTAGE=1.5V			MIN_LINE_WIDTH=15			MIN_NECK_WIDTH=6			12																																																																																																																																																																																																																																																																																						
					+1.5V_LDO			VOLTAGE=1.5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41							+1.5V INTREPID PLL6			VOLTAGE=1.5V			MIN_LINE_WIDTH=15			MIN_NECK_WIDTH=6			12																																																																																																																																																																																																																																																																																						
					+1.5V_SLEEP_VIN			VOLTAGE=1.5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41							+1.5V INTREPID PLL7			VOLTAGE=1.5V			MIN_LINE_WIDTH=15			MIN_NECK_WIDTH=6			8																																																																																																																																																																																																																																																																																						
		C	ADAPTER				+ADAPTER			VOLTAGE=24V			MIN_LINE_WIDTH=50			MIN_NECK_WIDTH=10			32 33 41			REFERENCE				INT MEM_VREF			VOLTAGE=1.25V			MIN_LINE_WIDTH=10			9																																																																																																																																																																																																																																																																																							
				+ADAPTER_SW			VOLTAGE=24V			MIN_LINE_WIDTH=50			MIN_NECK_WIDTH=10			40							INT AGP_VREF			VOLTAGE=1.25V			MIN_LINE_WIDTH=10			12 19																																																																																																																																																																																																																																																																																										
				+ADAPTER_SW			VOLTAGE=24V			MIN_LINE_WIDTH=50			MIN_NECK_WIDTH=10			40							INT MEM_REF_H			VOLTAGE=0V			MIN_LINE_WIDTH=10			9																																																																																																																																																																																																																																																																																										
				+ADAPTER_SENSE			VOLTAGE=24V			MIN_LINE_WIDTH=50			MIN_NECK_WIDTH=10			32							UIDE_REF			VOLTAGE=0V			MIN_LINE_WIDTH=8			13																																																																																																																																																																																																																																																																																										
B	BATTERY CHARGER				+BATT_POS			VOLTAGE=16.8V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			32 41			AIRPORT				+3V AIRPORT			VOLTAGE=3.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41																																																																																																																																																																																																																																																																																						
					BATT_NEG			VOLTAGE=0V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			41							+3V SLEEP_PCCARD			VOLTAGE=3.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			18																																																																																																																																																																																																																																																																																						
					+1772_DCIN			VOLTAGE=24V			MIN_LINE_WIDTH=10			32							+VCC_CBUS_SW			VOLTAGE=3.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			18																																																																																																																																																																																																																																																																																									
					+1772_LX			VOLTAGE=12.6V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			32							+VPP_CBUS_SW			VOLTAGE=5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			18																																																																																																																																																																																																																																																																																						
					+BATT_14V_FUSE			VOLTAGE=12.6V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			32							GPU_VCORE			VOLTAGE=1.2V			MIN_LINE_WIDTH=30			MIN_NECK_WIDTH=10			19 21 41																																																																																																																																																																																																																																																																																						
					+BATT_24V_FUSE			VOLTAGE=12.6V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			32							+3V_GPU			VOLTAGE=3.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			12 19 21 22																																																																																																																																																																																																																																																																																						
					+BATT_RSNS			VOLTAGE=12.6V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			32							+3V_GPU_FLT			VOLTAGE=3.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			22																																																																																																																																																																																																																																																																																						
					+BATT_VSNS			VOLTAGE=12.6V			MIN_LINE_WIDTH=10			MIN_NECK_WIDTH=10			32							+2.5V_GPU			VOLTAGE=2.5V			MIN_LINE_WIDTH=30			MIN_NECK_WIDTH=10			22																																																																																																																																																																																																																																																																																						
					+1772_LDO			VOLTAGE=5.4V			MIN_LINE_WIDTH=10			32							GPU_MEM_IO_FLT			VOLTAGE=2.5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			19 22																																																																																																																																																																																																																																																																																									
					+1772_DLOV			VOLTAGE=5.4V			MIN_LINE_WIDTH=10			32							+2.5V_GPU_MEMCORE			VOLTAGE=2.5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			22																																																																																																																																																																																																																																																																																									
					+1772_GND			VOLTAGE=0V			MIN_LINE_WIDTH=10			32							+1.8V_GPU			VOLTAGE=1.8V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			19 20 21 22																																																																																																																																																																																																																																																																																									
					+ADAPTER_ILIM			VOLTAGE=24V			MIN_LINE_WIDTH=10			33							+1.5V_AGP			VOLTAGE=1.5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			12 15 16 19 21 22																																																																																																																																																																																																																																																																																									
					+ADAPTER_OR_BATT			VOLTAGE=24V			MIN_LINE_WIDTH=10			33							+1.8V_ATI_PVDD			VOLTAGE=1.8V			MIN_LINE_WIDTH=20			MIN_NECK_WIDTH=10			21 22																																																																																																																																																																																																																																																																																									
					+4.85V_RAW			VOLTAGE=4.85V			MIN_LINE_WIDTH=10			31 33							+1.5V_AGP_GPU			VOLTAGE=1.5V			MIN_LINE_WIDTH=20			MIN_NECK_WIDTH=10			22																																																																																																																																																																																																																																																																																									
					+4.6V_BU			VOLTAGE=4.6V			MIN_LINE_WIDTH=10			33 34							+1.5V_GPU_VDD15			VOLTAGE=1.5V			MIN_LINE_WIDTH=20			MIN_NECK_WIDTH=10			21																																																																																																																																																																																																																																																																																									
					+4.85V_ESR			VOLTAGE=4.85V			MIN_LINE_WIDTH=10			33							+1.8V_GPU_PLL			VOLTAGE=1.8V			MIN_LINE_WIDTH=15			MIN_NECK_WIDTH=10			22																																																																																																																																																																																																																																																																																									
		A	MISC HD				+3V_PMU_ESR			VOLTAGE=3.3V			MIN_LINE_WIDTH=10			33			TRACKPAD					GPU_VCORE_VDDCI			VOLTAGE=1.2V			MIN_LINE_WIDTH=15			MIN_NECK_WIDTH=10			19																																																																																																																																																																																																																																																																																						
				+3V_PMU_AVCC			VOLTAGE=3.3V			MIN_LINE_WIDTH=10			27 31							+2.5V_GPU_A2VDD			VOLTAGE=2.5V			MIN_LINE_WIDTH=15			MIN_NECK_WIDTH=10			22																																																																																																																																																																																																																																																																																										
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																							+1.8V_GPU_MEMPLL			VOLTAGE=1.8V			MIN_LINE_WIDTH=10			MIN_NECK_WIDTH=10			22																																																																																																																																																																																																																																																																																							
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																							+GPU_VDD15_UP			VOLTAGE=1.5V			MIN_LINE_WIDTH=20			MIN_NECK_WIDTH=10			21																																																																																																																																																																																																																																																																																							
																							+2.5V_SLEEP_NECK1			VOLTAGE=2.5V			MIN_LINE_WIDTH=10			MIN_NECK_WIDTH=10			21																																																																																																																																																																																																																																																																																							
																							+3V_SLEEP_NECK			VOLTAGE=3V			MIN_LINE_WIDTH=10			MIN_NECK_WIDTH=10			36																																																																																																																																																																																																																																																																																							
																							+1.5V_AGP_NECK			VOLTAGE=1.5V			MIN_LINE_WIDTH=10			MIN_NECK_WIDTH=10			21																																																																																																																																																																																																																																																																																							
																							+1.8V_PVDD_NECK			VOLTAGE=1.8V			MIN_LINE_WIDTH=10			MIN_NECK_WIDTH=10			21																																																																																																																																																																																																																																																																																							
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A	AUDIO						+5V_MAIN_AUD			VOLTAGE=5V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10				27 34			ETHERNET				+2.5V_SLEEP_NECK2			VOLTAGE=2.5V			MIN_LINE_WIDTH=10			MIN_NECK_WIDTH=10			36																																																																																																																																																																																																																																																																																			
					+3V_MAIN_AUD			VOLTAGE=3.3V			MIN_LINE_WIDTH=25			MIN_NECK_WIDTH=10			27 34							+1.8V_SLEEP_NECK			VOLTAGE=1.8V			MIN_LINE_WIDTH=10			MIN_NECK_WIDTH=10			36																																																																																																																																																																																																																																																																																						
					+AUD_GND			VOLTAGE=0V			MIN_LINE_WIDTH=50			27						+1.5V_SLEEP_NECK				VOLTAGE=1.5V			MIN_LINE_WIDTH=10			MIN_NECK_WIDTH=10			36																																																																																																																																																																																																																																																																																									
																								+1.8V_ATI_TPVD			VOLTAGE=1.8V			MIN_LINE_WIDTH=20			MIN_NECK_WIDTH=10			22																																																																																																																																																																																																																																																																																						
																								+1.8V_GPU_TP_PLL			VOLTAGE=1.8V			MIN_LINE_WIDTH=15			MIN_NECK_WIDTH=10			22																																																																																																																																																																																																																																																																																						

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	REVISION HISTORY							
	EVT2 RELEASE							
D	08/13/04 - 1. CHANGE EXT TMDS SWING RESISTORS TO 510 OHM (R869, R876), REMOVE SI_RESET PULL HIGH 2. CHANGE RGB SIGNAL INPEDENCE (R341, R342, R346, R456, R458, R462) 3. ADD 2 RESISTORS (NO STUFF) BETWEEN FAN_PWM AND FAN_PWM_L OF FAN1 AND FAN2 4. CHANGE 2 CAPS (C233, C803) TO IMPROVE FEEDBACK PROTECTION AND PBUS CURRENT LIMIT CIRCUIT 5. MODIFY CPU_VCORE VID AND CPU_VCORE SETTING							
	08/16/04 - 1. MODIFY CPU_AVDD SETTING							
	08/20/04 - 1. ADD TRACKPAD POWER +5V_TPAD CONTROL CIRCUIT							
	09/01/04 - 1. CHANGE ALL FONTS INTO SMALL ONES							
	09/02/04 - 1. MODIFT CPU_VCORE VID AND CPU_VCORE SEETING AGAIN 2. MODIFY CPU_AVDD SEETING AGAIN							
	09/03/04 - 1. CHANGE INT TMDS DAMPING RESISTERS (R760-R767) TO 0 OHM 2. ADD MMM CIRCUIT, ARRANGE 2 INTREPID GPIOS FOR MM_FFIRQ_L, MM_SIRQ_L AND PULL UP RESISTORS R801, R802 3. ADD R803 BETWEEN DP6 AND DCDC_IN 4. ADD R804 AND SUPERCAP C692 ON +4_6V_BU 5. CHANGE TRACKPAD CONNECTOR J10 AND PIN OUT							
	09/06/04 - 1. ADD EMI SOLUTION L12							
	09/07/04 - 1. CHANGE TRACKPAD CONNECTOR PIN OUT							
	09/08/04 - 1. ADD BATTERY CURRENT SENSOR CIRCUIT							
	09/09/04 - 1. ADD EMI SOLUTION R816; ADD MMM RESET CIRCUIT							
C	09/10/04 - 1. MODIFY FIREWIRE PORT0 POWER CIRCUIT 2. ADD NET FROM BATTERY CURRENT SENSOR CIRCUIT TO PMU							
	09/13/04 - 1. ADD CURRENT LIMITER R821 BETWEEN PMU(U29) AND U33 2. ADD PULL UP AND PULL DOWN RESISTORS FOR MMM SENSOR							
	DVT RELEASE							
	09/27/04 - 1. ADD ST MMM SENSOR CIRCUIT							
	10/14/04 - 2. ADD FIREWIRE POWER PROTECT CIRCUIT							
	10/15/04 - 3. CHANGE EXT_TMDS TERMINAL RESISTERS AND V SWINING RESISTOR							
	10/22/04 - 4. CHANGE FAN CONTROLLER FROM ADT7460 TO ADT7467							
	11/02/04 - 5. CHANGE BBANG IC TO ATTINY2313							
	PVT RELEASE							
	12/17/04 - 1. REMOVE ALL OPEN JUMPER							
	12/17/04 - 2. SCHEMATIC RELEASE FOR PRODUCTION							
B	PVT RELEASE (REV C)							
	02/11/05 - 1. CHANGE FW F3 TO 740S0018							
	PRODUCTION RELEASE (REV D)							
	04/12/05 - 1. ADD MPU R1.4 2. CHANGE 88E1111 B1(338S0223) TO PRIMARY AND B0 (338S0079) TO SECONDARY							
	PRODUCTION RELEASE (REV E)							
	08/24/05 - 1. ADD MPU R1.5 (337S3217 AND 337S3218)							
	08/25/05 - 1. ADD 341S1792 (BOOTROM,4.9.1F3)							
A								
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	<div>APPLE COMPUTER INC.</div>		<div>SIZE</div> D	<div>DRAWING NUMBER</div> 051-6680		<div>REV.</div> E		
			<div>SCALE</div> NONE		<div>SHT</div> 42	<div>OF</div> 46		
	8	7	6	5	4	3	2	1


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